Difmicro Technolog

DIF81F932

Datasheet

Content

DIF81F932 Product characteristics

● Special Microcontroller Features:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC–20 MHz oscillator/clock input
  - DC–200 ns instruction cycle
- Program Memory Read (PMR) capability
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

● Special single chip microcomputer function:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - External Oscillator fail detect for critical applications
  - Clock mode switching during operation for power savings
- Software selectable 31 kHz internal oscillator
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years

● Low-Power Features:

- Standby Current:
  - <100 nA @ 2.0V, typical
- Operating Current:
  - 11 uA @ 32 kHz, 2.0V, typical
  - 220 uA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 uA @ 2.0V, typical

Peripheral Features

- Liquid Crystal Display module:
  - Up to 60/96/168 pixel drive capability on 28/40/64-pin devices, respectively
  - Four commons
- Up to 24/35/53 I/O pins and 1 input-only pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-change pin
  - Individually programmable weak pull-ups
- In-Circuit Serial Programming (ICSP) via two pins
- Analog comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- A/D Converter:
  - 10-bit resolution and up to 8 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 as Timer1 oscillator if INTOSCIO or LP mode is selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Up to 2 Capture, Compare, PWM modules:
  - 16-bit Capture, max. resolution 12.5 ns
  - 16-bit Compare, max. resolution 200 ns
  - 10-bit PWM, max. frequency 20 kHz
- Synchronous Serial Port (SSP) with I2C

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	LCD (segment drivers)	CCP	Timers 8/16-bit
	Flash (words/bytes)	SRAM (bytes)	EEPROM (bytes)					
DIF81F932	4K/7K	256	256	35	8	24	2	2/1

Pin Diagram

DIF81F932DI, 40-pin DIP

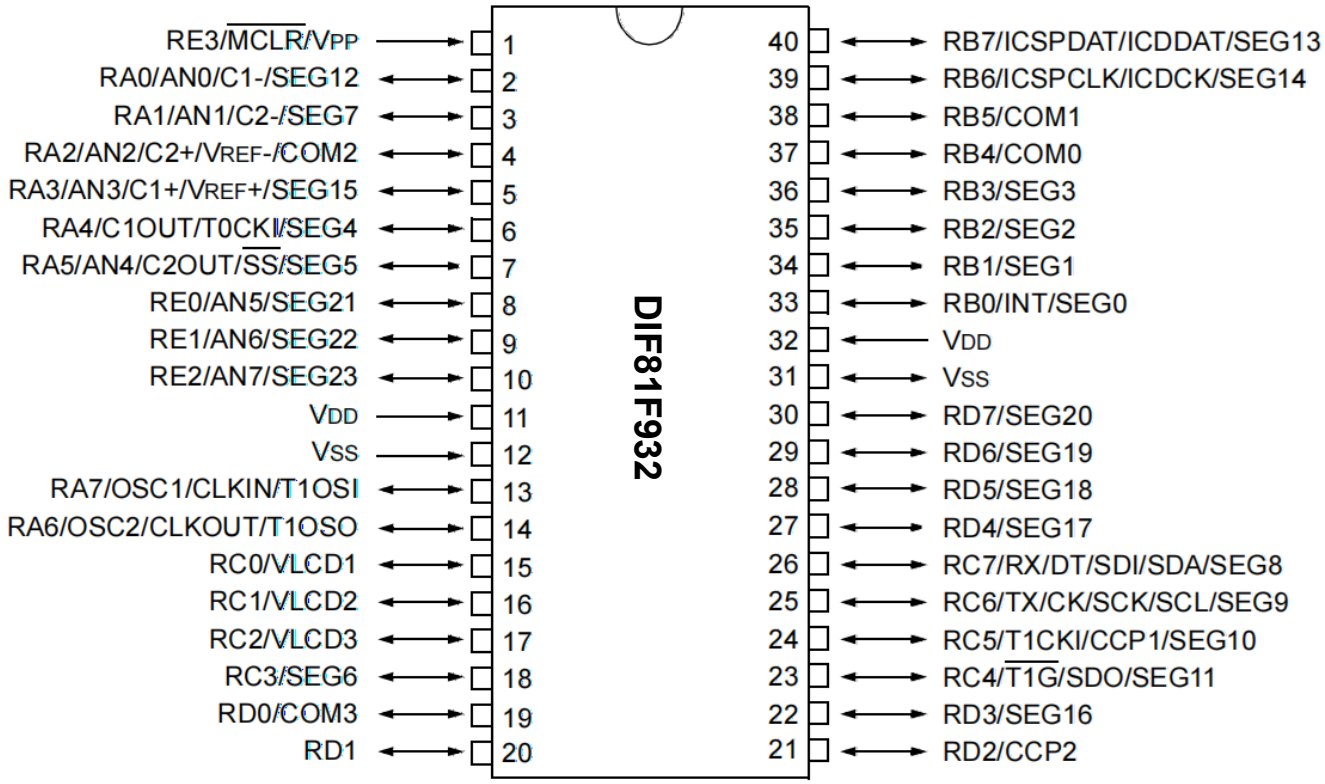


Table 1. DIF81F932 40-PIN SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	3	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	4	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	5	AN3/VREF+	SEG15	C1+	—	—	—	—	—	—	—
RA4	6		SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	7	AN4	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	14	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	13	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	33	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	34	—	SEG1	—	—	—	—	—	—	Y	—
RB2	35	—	SEG2	—	—	—	—	—	—	Y	—
RB3	36	—	SEG3	—	—	—	—	—	—	Y	—
RB4	37	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	38	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	39	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	40	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	15	—	VLCD1	—	—	—	—	—	—	—	—
RC1	16	—	VLCD2	—	—	—	—	—	—	—	—
RC2	17	—	VLCD3	—	—	—	—	—	—	—	—
RC3	18	—	SEG6	—	—	—	—	—	—	—	—
RC4	23	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	24	—	SEG10	—	T1CKI	CCP1	—		—	—	—
RC6	25	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	26	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RD0	19	—	COM3	—	—	—	—	—	—	—	—
RD1	20	—	—	—	—	—	—	—	—	—	—
RD2	21	—	—	—	—	CCP2	—	—	—	—	—
RD3	22	—	SEG16	—	—	—	—	—	—	—	—
RD4	27	—	SEG17	—	—	—	—	—	—	—	—
RD5	28	—	SEG18	—	—	—	—	—	—	—	—
RD6	29	—	SEG19	—	—	—	—	—	—	—	—
RD7	30	—	SEG20	—	—	—	—	—	—	—	—
RE0	8	AN5	SEG21	—	—	—	—	—	—	—	—
RE1	9	AN6	SEG22	—	—	—	—	—	—	—	—
RE2	10	AN7	SEG23	—	—	—	—	—	—	—	—
RE3	1	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	11	—	—	—	—	—	—	—	—	—	VDD
—	32	—	—	—	—	—	—	—	—	—	VDD
—	12	—	—	—	—	—	—	—	—	—	VSS
—	31	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up activated only with external $\overline{MCLR}$ configuration.

DIF81F932QI, 44-pin QFP

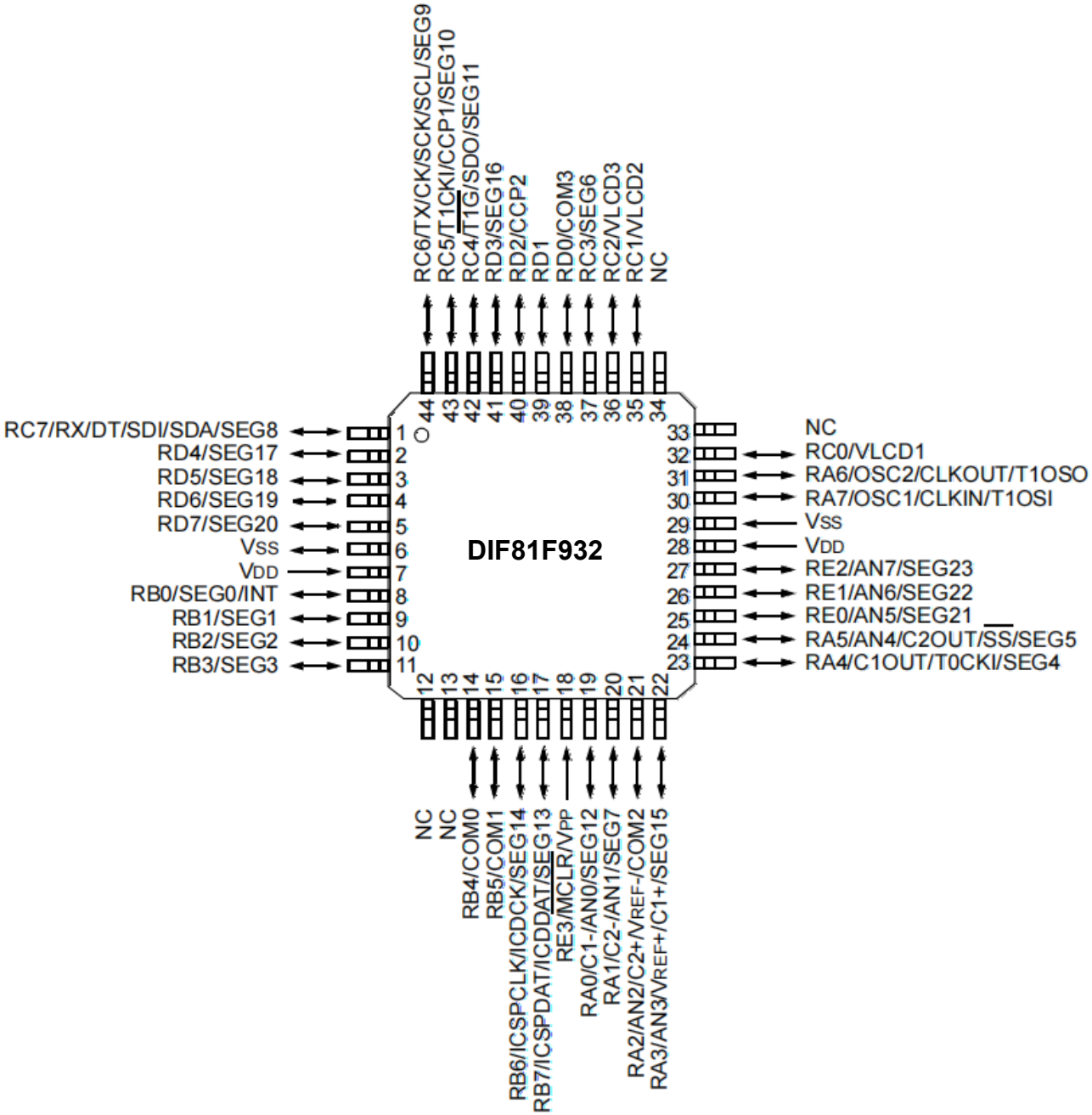


Table 2. DIF81F932 44-PIN(QFP) SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	19	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	20	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	21	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	22	AN3/VREF+	SEG15	C1+	—	—	—	—	—	—	—
RA4	23	—	SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	24	AN4	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	31	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	30	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	8	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	9	—	SEG1	—	—	—	—	—	—	Y	—
RB2	10	—	SEG2	—	—	—	—	—	—	Y	—
RB3	11	—	SEG3	—	—	—	—	—	—	Y	—
RB4	14	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	15	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	16	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	17	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	32	—	VLCD1	—	—	—	—	—	—	—	—
RC1	35	—	VLCD2	—	—	—	—	—	—	—	—
RC2	36	—	VLCD3	—	—	—	—	—	—	—	—
RC3	37	—	SEG6	—	—	—	—	—	—	—	—
RC4	42	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	43	—	SEG10	—	T1CKI	CCP1	—	—	—	—	—
RC6	44	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	1	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RD0	38	—	COM3	—	—	—	—	—	—	—	—
RD1	39	—	—	—	—	—	—	—	—	—	—
RD2	40	—	—	—	—	CCP2	—	—	—	—	—
RD3	41	—	SEG16	—	—	—	—	—	—	—	—
RD4	2	—	SEG17	—	—	—	—	—	—	—	—
RD5	3	—	SEG18	—	—	—	—	—	—	—	—
RD6	4	—	SEG19	—	—	—	—	—	—	—	—
RD7	5	—	SEG20	—	—	—	—	—	—	—	—
RE0	25	AN5	SEG21	—	—	—	—	—	—	—	—
RE1	26	AN6	SEG22	—	—	—	—	—	—	—	—
RE2	27	AN7	SEG23	—	—	—	—	—	—	—	—
RE3	18	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	7	—	—	—	—	—	—	—	—	—	VDD
—	28	—	—	—	—	—	—	—	—	—	VDD
—	6	—	—	—	—	—	—	—	—	—	VSS
—	29	—	—	—	—	—	—	—	—	—	VSS
—	12	—	—	—	—	—	—	—	—	—	NC
—	13	—	—	—	—	—	—	—	—	—	NC
—	33	—	—	—	—	—	—	—	—	—	NC
—	34	—	—	—	—	—	—	—	—	—	NC

Note 1: Pull-up activated only with external $\overline{MCLR}$ configuration.

CPU Kernel

DEVICE OVERVIEW

The DIF81F932 devices are covered by this data sheet. They are available in 40/44-pin packages. ***Figure 1*** shows a block diagram of the DIF81F932 device. ***Table 3*** shows the pinout descriptions.

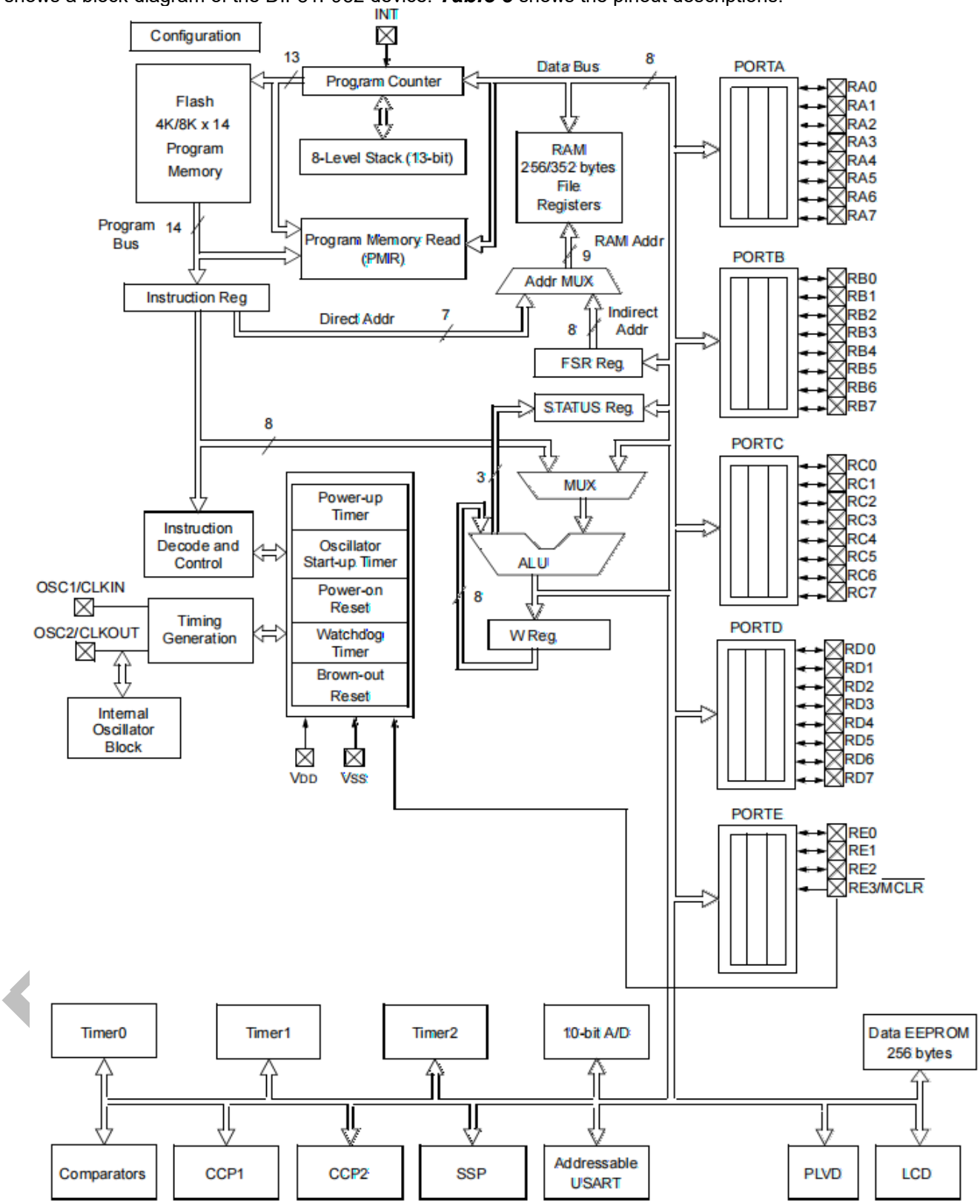


Figure 1.DIF81F932 BLOCK DIAGRAM

Table 3.DIF81F932 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1-/SEG12	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	Analog input Channel 0.
	C1-	AN	—	Comparator 1 negative input.
	SEG12	—	AN	LCD analog output.
RA1/AN1/C2-/SEG7	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	Analog input Channel 1.
	C2-	AN	—	Comparator 2 negative input.
	SEG7	—	AN	LCD analog output.
RA2/AN2/C2+/VREF-/COM2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	Analog input Channel 2.
	C2+	AN	—	Comparator 2 positive input.
	VREF-	AN	—	External A/D Voltage Reference – negative.
	COM2	—	AN	LCD analog output.
RA3/AN3/C1+/VREF+/COM3(1)/ SEG15	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	Analog input Channel 3.
	C1+	AN	—	Comparator 1 positive input.
	VREF+	AN	—	External A/D Voltage Reference – positive.
	COM3(1)	—	AN	LCD analog output.
	SEG15	—	AN	LCD analog output.
RA4/C1OUT/T0CKI/SEG4	RA4	TTL	CMOS	General purpose I/O.
	C1OUT	—	CMOS	Comparator 1 output.
	T0CKI	ST	—	Timer0 clock input.
	SEG4	—	AN	LCD analog output.
$\overline{RA5}$/AN4/C2OUT/SS/SEG5	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	Analog input Channel 4.
	C2OUT	—	CMOS	Comparator 2 output.
	$\overline{SS}$	TTL	—	Slave select input.
	SEG5	—	AN	LCD analog output.
RA6/OSC2/CLKOUT/T1OSO	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
	T1OSO	—	XTAL	Timer1 oscillator output.
RA7/OSC1/CLKIN/T1OSI	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	Clock input.
	T1OSI	XTAL	—	Timer1 oscillator input.
RB0/INT/SEG0	RB0	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	INT	ST	—	External interrupt pin.
	SEG0	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the DIF81F932/916 and on RD0 for the DIF81F932 and DIF81F964S.

2: Pins available on DIF81F932 and DIF81F964S only.

3: Pins available on DIF81F964S only.

4: I2C Schmitt trigger inputs have special input levels.

Name	Function	Input Type	Output Type	Description
RB1/SEG1	RB1	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG1	—	AN	LCD analog output.
RB2/SEG2	RB2	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG2	—	AN	LCD analog output.
RB3/SEG3	RB3	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG3	—	AN	LCD analog output.
RB4/COM0	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	COM0	—	AN	LCD analog output.
RB5/COM1	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	COM1	—	AN	LCD analog output.
RB6/ICSPCLK/ICDCK/SEG14	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	ICSP clock.
	ICDCK	ST	—	ICD clock.
	SEG14	—	AN	LCD analog output.
RB7/ICSPDAT/ICDDAT/SEG13	RB7	TTL	CMOS	General purpose I/O. Individually controlled inter- rupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP Data I/O.
	ICDDAT	ST	CMOS	ICD Data I/O.
	SEG13	—	AN	LCD analog output.
RC0/VLCD1	RC0	ST	CMOS	General purpose I/O.
	VLCD1	AN	—	LCD analog input.
RC1/VLCD2	RC1	ST	CMOS	General purpose I/O.
	VLCD2	AN	—	LCD analog input.
RC2/VLCD3	RC2	ST	CMOS	General purpose I/O.
	VLCD3	AN	—	LCD analog input.
RC3/SEG6	RC3	ST	CMOS	General purpose I/O.
	SEG6	—	AN	LCD analog output.
$\overline{\text{RC4}}$/T1G/SDO/SEG11	RC4	ST	CMOS	General purpose I/O.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate input.
	SDO	—	CMOS	Serial data output.
	SEG11	—	AN	LCD analog output.
RC5/T1CKI/CCP1/SEG10	RC5	ST	CMOS	General purpose I/O.
	T1CKI	ST	—	Timer1 clock input.
	CCP1	ST	CMOS	Capture 1 input/Compare 1 output/PWM 1 output.
	SEG10	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the DIF81F932/916 and on RD0 for the DIF81F932 and DIF81F964S.

2: Pins available on DIF81F932 and DIF81F964S only.

3: Pins available on DIF81F964S only.

4: I2C Schmitt trigger inputs have special input levels.

Name	Function	Input Type	Output Type	Description
RC6/TX/CK/SCK/SCL/SEG9	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous serial transmit.
	CK	ST	CMOS	USART synchronous serial clock.
	SCK	ST	CMOS	SPI clock.
	SCL	ST(4)	OD	I^2C clock.
	SEG9	—	AN	LCD analog output.
RC7/RX/DT/SDI/SDA/SEG8	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous serial receive.
	DT	ST	CMOS	USART synchronous serial data.
	SDI	ST	CMOS	SPI data input.
	SDA	ST(4)	OD	I^2C data.
	SEG8	—	AN	LCD analog output.
RD0/COM3(1, 2)	RD0	ST	CMOS	General purpose I/O.
	COM3	—	AN	LCD analog output.
RD1(2)	RD1	ST	CMOS	General purpose I/O.
RD2/CCP2(2)	RD2	ST	CMOS	General purpose I/O.
	CCP2	ST	CMOS	Capture 2 input/Compare 2 output/PWM 2 output.
RD3/SEG16(2)	RD3	ST	CMOS	General purpose I/O.
	SEG16	—	AN	LCD analog output.
RD4/SEG17(2)	RD4	ST	CMOS	General purpose I/O.
	SEG17	—	AN	LCD analog output.
RD5/SEG18(2)	RD5	ST	CMOS	General purpose I/O.
	SEG18	—	AN	LCD analog output.
RD6/SEG19(2)	RD6	ST	CMOS	General purpose I/O.
	SEG19	—	AN	LCD analog output.
RD7/SEG20(2)	RD7	ST	CMOS	General purpose I/O.
	SEG20	—	AN	LCD analog output.
RE0/AN5/SEG21(2)	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	Analog input Channel 5.
	SEG21	—	AN	LCD analog output.
RE1/AN6/SEG22(2)	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	Analog input Channel 6.
	SEG22	—	AN	LCD analog output.
RE2/AN7/SEG23(2)	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	Analog input Channel 7.
	SEG23	—	AN	LCD analog output.
$\overline{\text{RE3}}$/$\overline{\text{MCLR}}$/V_{PP}	RE3	ST	—	Digital input only.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the DIF81F932/916 and on RD0 for the DIF81F932 and DIF81F964S.

2: Pins available on DIF81F932 and DIF81F964S only.

3: Pins available on DIF81F964S only.

4: I2C Schmitt trigger inputs have special input levels.

Name	Function	Input Type	Output Type	Description
RE4/SEG24(3)	RE4	ST	CMOS	General purpose I/O.
	SEG24	—	AN	LCD analog output.
RE5/SEG25(3)	RE5	ST	CMOS	General purpose I/O.
	SEG25	—	AN	LCD analog output.
RE6/SEG26(3)	RE6	ST	CMOS	General purpose I/O.
	SEG26	—	AN	LCD analog output.
RE7/SEG27(3)	RE7	ST	CMOS	General purpose I/O.
	SEG27	—	AN	LCD analog output.
RF0/SEG32(3)	RF0	ST	CMOS	General purpose I/O.
	SEG32	—	AN	LCD analog output.
RF1/SEG33(3)	RF1	ST	CMOS	General purpose I/O.
	SEG33	—	AN	LCD analog output.
RF2/SEG34(3)	RF2	ST	CMOS	General purpose I/O.
	SEG34	—	AN	LCD analog output.
RF3/SEG35(3)	RF3	ST	CMOS	General purpose I/O.
	SEG35	—	AN	LCD analog output.
RF4/SEG28(3)	RF4	ST	CMOS	General purpose I/O.
	SEG28	—	AN	LCD analog output.
RF5/SEG29(3)	RF5	ST	CMOS	General purpose I/O.
	SEG29	—	AN	LCD analog output.
RF6/SEG30(3)	RF6	ST	CMOS	General purpose I/O.
	SEG30	—	AN	LCD analog output.
RF7/SEG31(3)	RF7	ST	CMOS	General purpose I/O.
	SEG31	—	AN	LCD analog output.
RG0/SEG36(3)	RG0	ST	CMOS	General purpose I/O.
	SEG36	—	AN	LCD analog output.
RG1/SEG37(3)	RG1	ST	CMOS	General purpose I/O.
	SEG37	—	AN	LCD analog output.
RG2/SEG38(3)	RG2	ST	CMOS	General purpose I/O.
	SEG38	—	AN	LCD analog output.
RG3/SEG39(3)	RG3	ST	CMOS	General purpose I/O.
	SEG39	—	AN	LCD analog output.
RG4/SEG40(3)	RG4	ST	CMOS	General purpose I/O.
	SEG10	—	AN	LCD analog output.
RG5/SEG41(3)	RG5	ST	CMOS	General purpose I/O.
	SEG41	—	AN	LCD analog output.
AV_{DD}(3)	AVDD	P	—	Analog power supply for microcontroller.
AV_{SS}(3)	AVSS	P	—	Analog ground reference for microcontroller.
V_{DD}	VDD	P	—	Power supply for microcontroller.
VSS	VSS	P	—	Ground reference for microcontroller.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the DIF81F932/916 and on RD0 for the DIF81F932 and DIF81F964S.

2: Pins available on DIF81F932 and DIF81F964S only.

3: Pins available on DIF81F964S only.

4: I2C Schmitt trigger inputs have special input levels.

MEMORY ORGANIZATION

Program Memory Organization

The DIF81F932 has a 13-bit program counter capable of addressing a 4K x 14 program memory space for the DIF81F932 (0000h-0FFFh). Accessing a location above the memory boundaries for the DIF81F932 will cause a wrap around within the first 4K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

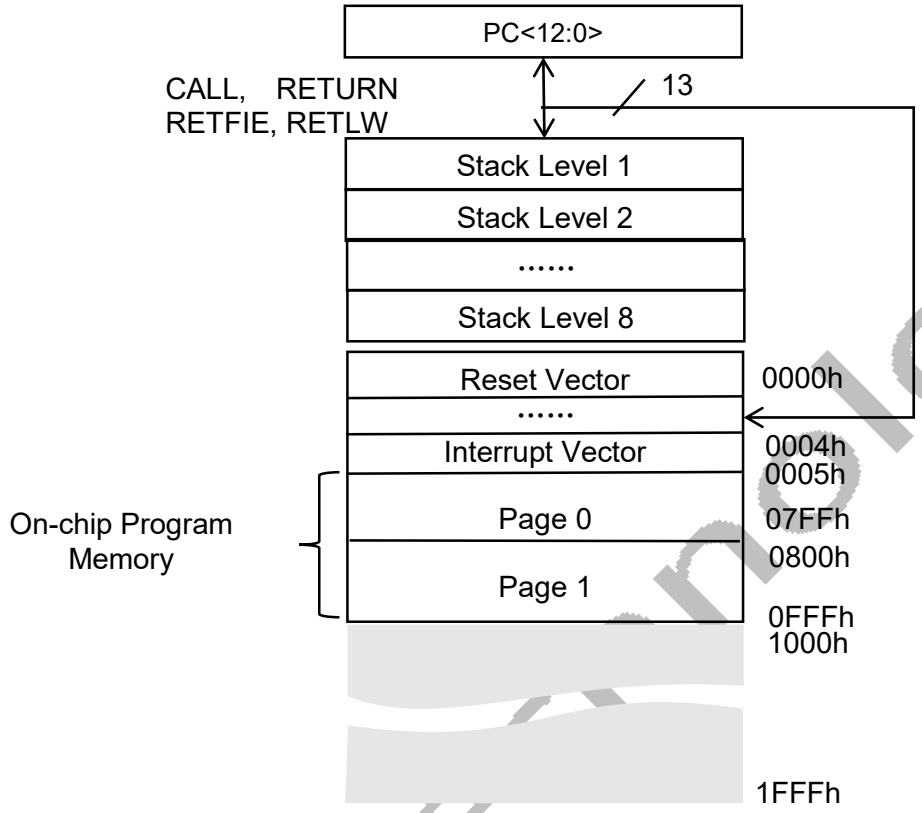


Figure 2. PROGRAM MEMORY MAP AND STACK FOR THE DIF81F932

Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 bits in the DIF81F932. Each register is accessed either directly or indirectly through the File Select Register (FSR).

SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

	File Address		File Address		File Address		File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h		187h
PORTD	08h	TRISD	88h	LCDPS	108h		188h
PORTE	09h	TRISE	89h	LVDCON	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h		190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h		
T2CON	12h	PR2	92h	LCDDATA2	112h		
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h		
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h		
CCPR1L	15h	WPUB	95h	LCDDATA5	115h		
CCPR1H	16h	IOCB	96h	LCDDATA6	116h		
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h		
RCSTA	18h	TXSTA	98h	LCDDATA8	118h		
TXREG	19h	SPBRG	99h	LCDDATA9	119h		
RCREG	1Ah		9Ah	LCDDATA10	11Ah	General Purpose Register(2)	
CCPR2L	1Bh		9Bh	LCDDATA11	11Bh		
CCPR2H	1Ch	CMCON0	9Ch	LCDSE0	11Ch	96 Bytes	
CCP2CON	1Dh	VRCON	9Dh	LCDSE1	11Dh		
ADRESH	1Eh	ADRESL	9Eh	LCDSE2	11Eh		
ADCON0	1Fh	ADCON1	9Fh		11Fh		
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h		
	7Fh		EFh		16Fh		1EFh
accesses 70h-7Fh		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F0h
			FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Figure 3. DIF81F932 SPECIAL FUNCTION REGISTERS

☐ Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: On the DIF81F932, unimplemented data memory locations, read as '0'.

Table 4. DIF81F932 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 0										
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx
08h	PORTD(2)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx
09h	PORTE	RE7(3)	RE6(3)	RE5(3)	RE4(3)	RE3	RE2(2)	RE1(2)	RE0(2)	xxxx xxxx
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
0Ch	PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000
0Dh	PIR2	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF(2)	0000 -0-0
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000
11h	TMR2	Timer2 Module Register								0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x
19h	TXREG	USART Transmit Data Register								0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000
1Bh(2)	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx
1Ch(2)	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx
1Dh(2)	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx
1Fh	ADCON0	ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	$\overline{GO/DONE}$	ADON	0000 0000

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (NON Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: DIF81F932 only.

3: forced to '0' on DIF81F932.

Table 5. DIF81F932 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 1										
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111
88h	TRISD(3)	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111
89h	TRISE	TRISE7(2)	TRISE6(2)	TRISE5(2)	TRISE4(2)	TRISE3(5)	TRISE2(3)	TRISE1(3)	TRISE0(3)	1111 1111
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
8Ch	PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000
8Dh	PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE(3)	0000 -0-0
8Eh	PCON	—	—	—	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$	---1 --qq
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS(4)	HTS	LTS	SCS	-110 q000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000
91h	ANSEL	ANS7(3)	ANS6(3)	ANS5(3)	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111
92h	PR2	Timer2 Period Register								1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000
94h	SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	0000 ----
97h	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010
99h	SPBRG	SPBRG7	SPBRG6	SPBRG5	SPBRG4	SPBRG3	SPBRG2	SPBRG1	SPBRG0	0000 0000
9Ah	—	Unimplemented								—
9Bh	—	Unimplemented								—
9Ch	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000
9Dh	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (NON Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: forced '0' on DIF81F932.

3: DIF81F932 only.

4: The value of the OSTS bit is dependent on the value of the Configuration Word (CONFIG) of the device.

5: Bit is read-only; TRISE3 = 1 always.

Table 6. DIF81F932 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 2										
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
101h	TMR0	Timer0 Module Register								xxxx xxxx
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
105h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx
107h	LCDCON	LCDEN	$\overline{SLPEN}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011
108h	LCDPS	WFT	BIASMD	LCDA	WA	LP3	LP2	LP1	LP0	0000 0000
109h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -100
10Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
10Ch	EEDATL	EEDATL7	EEDATL6	EEDATL5	EEDATL4	EEDATL3	EEDATL2	EEDATL1	EEDATL0	0000 0000
10Dh	EEADRL	EEADRL7	EEADRL6	EEADRL5	EEADRL4	EEADRL3	EEADRL2	EEADRL1	EEADRL0	0000 0000
10Eh	EEDATH	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000
10Fh	EEADRH	—	—	—	EEADRH4	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---0 0000
110h	LCDDATA0	SEG7 COM0	SEG6 COM0	SEG5 COM0	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0	xxxx xxxx
111h	LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0	xxxx xxxx
112h	LCDDATA2(2)	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	xxxx xxxx
113h	LCDDATA3	SEG7 COM1	SEG6 COM1	SEG5 COM1	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1	xxxx xxxx
114h	LCDDATA4	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1	xxxx xxxx
115h	LCDDATA5(2)	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	xxxx xxxx
116h	LCDDATA6	SEG7 COM2	SEG6 COM2	SEG5 COM2	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2	xxxx xxxx
117h	LCDDATA7	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2	xxxx xxxx
118h	LCDDATA8(2)	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	xxxx xxxx
119h	LCDDATA9	SEG7 COM3	SEG6 COM3	SEG5 COM3	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3	xxxx xxxx
11Ah	LCDDATA10	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3	xxxx xxxx
11Bh	LCDDATA11(2)	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	xxxx xxxx
11Ch	LCDSE0(3)	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	0000 0000
11Dh	LCDSE1(3)	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000
11Eh	LCDSE2(2,3)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000
11Fh	—	Unimplemented								—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (NON Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.
2: DIF81F932 only.
3: This register is only initialized by a POR or BOR reset and is unchanged by other Resets.

Table 7. DIF81F932 SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 3										
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
182h	PCL	Program Counter (PC) Least Significant Byte								0000 0000
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
184h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
185h	TRISF(3)	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	1111 1111
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
187h	TRISG(3)	—	—	TRISG5	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	--11 1111
188h	PORTF(3)	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx xxxx
189h	PORTG(3)	—	—	RG5	RG4	RG3	RG2	RG1	RG0	--xx xxxx
18Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	0--- x000
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----
18Eh	—	Reserved								—
18Fh	—	Reserved								—
190h	LCDDATA12(3)	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0	xxxx xxxx
191h	LCDDATA13(3)	SEG39 COM0	SEG38 COM0	SEG37 COM0	SEG36 COM0	SEG35 COM0	SEG34 COM0	SE33 COM0	SEG32 COM0	xxxx xxxx
192h	LCDDATA14(3)	—	—	—	—	—	—	SEG41 COM0	SEG40 COM0	---- --xx
193h	LCDDATA15(3)	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1	xxxx xxxx
194h	LCDDATA16(3)	SEG39 COM1	SEG38 COM1	SEG37 COM1	SEG36 COM1	SEG35 COM1	SEG34 COM1	SEG33 COM1	SEG32 COM1	xxxx xxxx
195h	LCDDATA17(3)	—	—	—	—	—	—	SEG41 COM1	SEG40 COM1	---- --xx
196h	LCDDATA18(3)	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2	xxxx xxxx
197h	LCDDATA19(3)	SEG39 COM2	SEG38 COM2	SEG37 COM2	SEG36 COM2	SEG35 COM2	SEG34 COM2	SEG33 COM2	SEG32 COM2	xxxx xxxx
198h	LCDDATA20(3)	—	—	—	—	—	—	SEG41 COM2	SEG40 COM2	---- --xx
199h	LCDDATA21(3)	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3	xxxx xxxx
19Ah	LCDDATA22(3)	SEG39 COM3	SEG38 COM3	SEG37 COM3	SEG36 COM3	SEG35 COM3	SEG34 COM3	SEG33 COM3	SEG32 COM3	xxxx xxxx
19Bh	LCDDATA23(3)	—	—	—	—	—	—	SEG41 COM3	SEG40 COM3	---- --xx
19Ch	LCDSE3(2, 3)	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000
19Dh	LCDSE4(2, 3)	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	0000 0000
19Eh	LCDSE5(2, 3)	—	—	—	—	—	—	SE41	SE40	---- --00
19Fh	—	Unimplemented								—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (NON Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.
2: This register is only initialized by a POR or BOR reset and is unchanged by other Resets.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias.....-40°C to+125°C
Storage temperature.....-65°C to+150°C
Voltage on VDD with respect to VSS.....-0.3to+6.5V
Voltage on MCLR with respect to Vss.....-0.3to +13.5V
Voltage on all other pins with respect to VSS.....-0.3V to (VDD + 0.3V)
Total power dissipation (1).....800mW
Maximum current out of V_{SS} pin.....95mA
Maximum current into V_{DD} pin.....95mA
Input clamp current, IIK (V_I < 0 or V_I > V_{DD}).....±20 mA
Output clamp current, IOK (V_o < 0 or Vo >V_{DD}).....±20 mA
Maximum output current sunk by any I/O pin.....25 mA
Maximum output current sourced by any I/O pin.....25 mA
Maximum current sunk by PORTA, PORTB and PORTC 90mA
Maximum current sourced PORTA, PORTB and PORTC 90mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

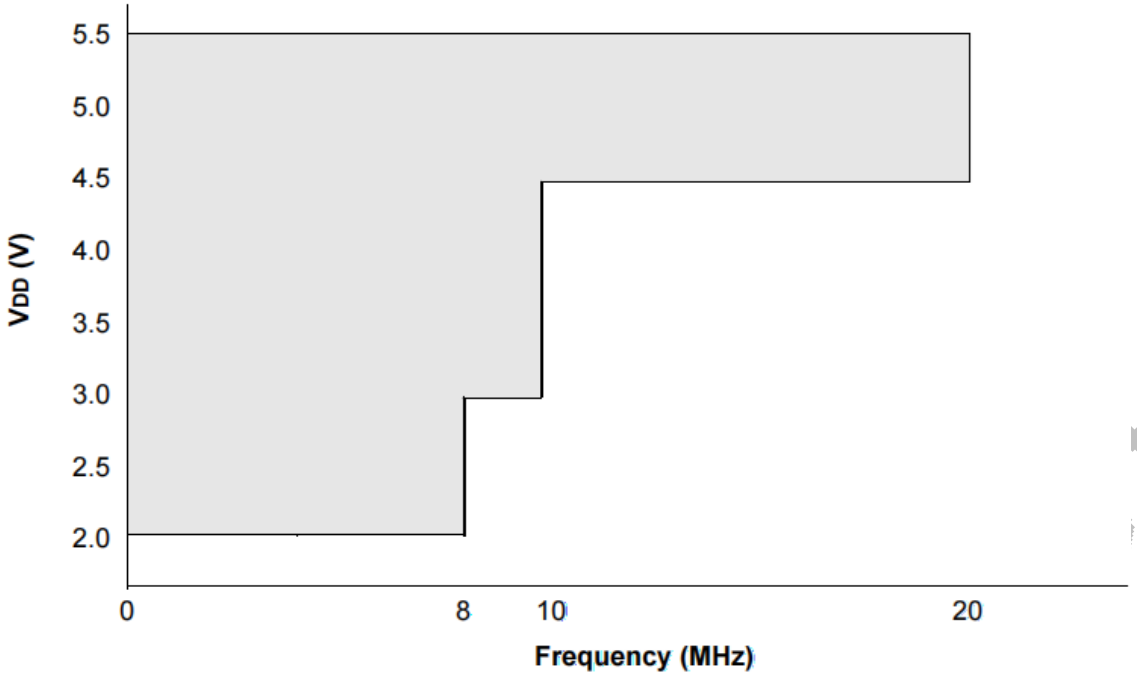


Figure 4. DIF81F932 VOLTAGE-FREQUENCY GRAPH, -40°C≤TA≤+125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

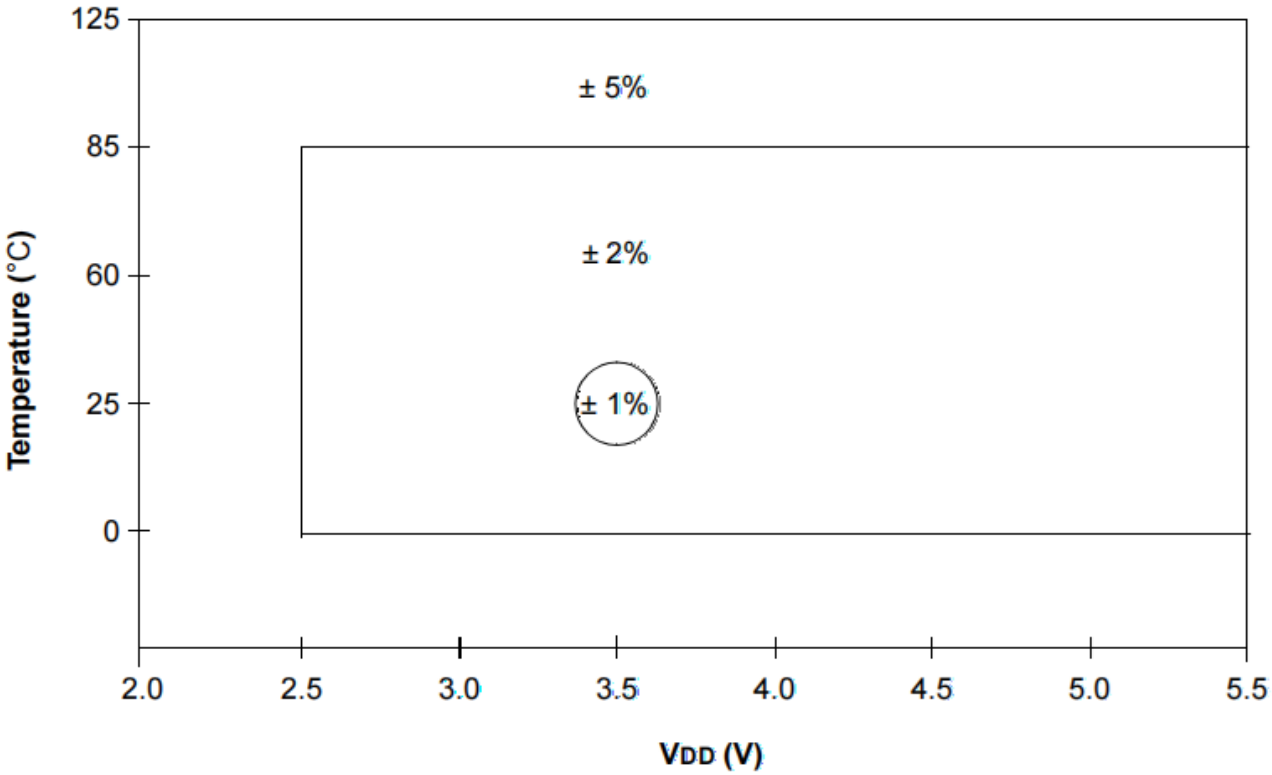


Figure 5. HFINTOSC FREQUENCY ACCURACY OVER DEVICE V_{DD} AND TEMPERATURE

DC Characteristics: DIF81F932

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001 D001C D001D	VDD	**Supply Voltage**	2.0 2.0 3.0 4.5	— — — —	5.5 5.5 5.5 5.5	V V V V	FOSC < = 8 MHz: HFINTOSC, EC FOSC < = 4 MHz FOSC < = 10 MHz FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	

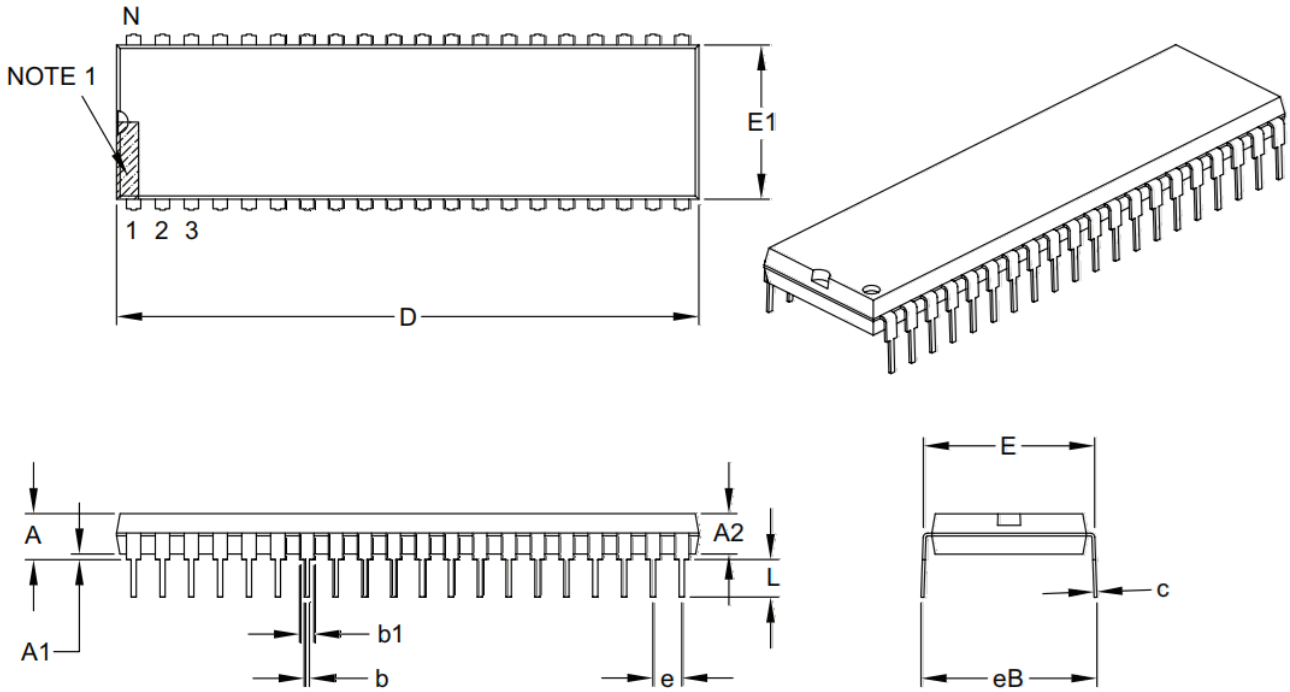
* These parameters are characterized but not tested.

† Data in "Type" column is at 5.0V, 25° C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

Package Details

DIF81F932DI, 40-Lead Plastic Dual In-Line (P)-600 mil Body [DIP]



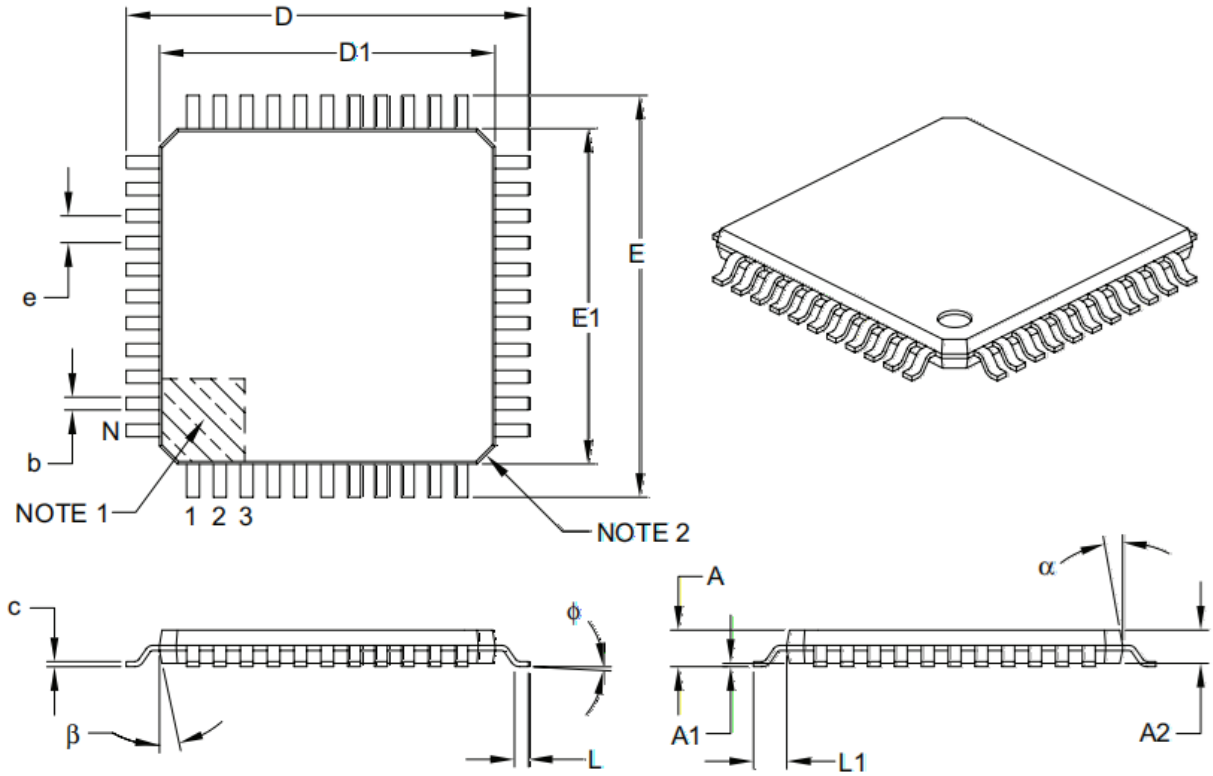
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F932QI, 44-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [QFP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.