Difmicro Technolog

DIF81F707

Datasheet

Content

DIF81F707 Product characteristics

● Special Microcontroller Features:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC - 20 MHz oscillator/clock input
  - DC - 200 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack Direct, Indirect and Relative Addressing modes

● Special single chip microcomputer function:

- Precision Internal Oscillator:
  - Factory calibrated to ± 1%
  - Software selectable frequency range of 8 MHz to 32 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide Operating Voltage Range (2.0V-5.5V)
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRTE) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Software Control Option
- Enhanced Low-Current Watchdog Timer (WDT) with On-Chip Oscillator (Software select able nominal 268 Seconds with Full Prescaler) with Software Enable
- Multiplexed Master Clear/Input Pin
- Programmable Code Protection
- High Endurance Flash/EEPROM Cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years
- Enhanced USART Module:
  - Supports RS-485, RS-232 and LIN 2.0
  - Auto-Baud Detect
  - Auto-wake-up on Start bit

● Low-Power Features:

- Operating Current:
  - 11A @ 32 kHz, 2.0V, typical
  - 220A@ 4 MHz, 2.0V, typical
- Standby Current:
  - 50nA @ 2.0V, typical
- Watchdog Timer Current:
  - <1A @ 2.0V, typical

● Peripheral Features

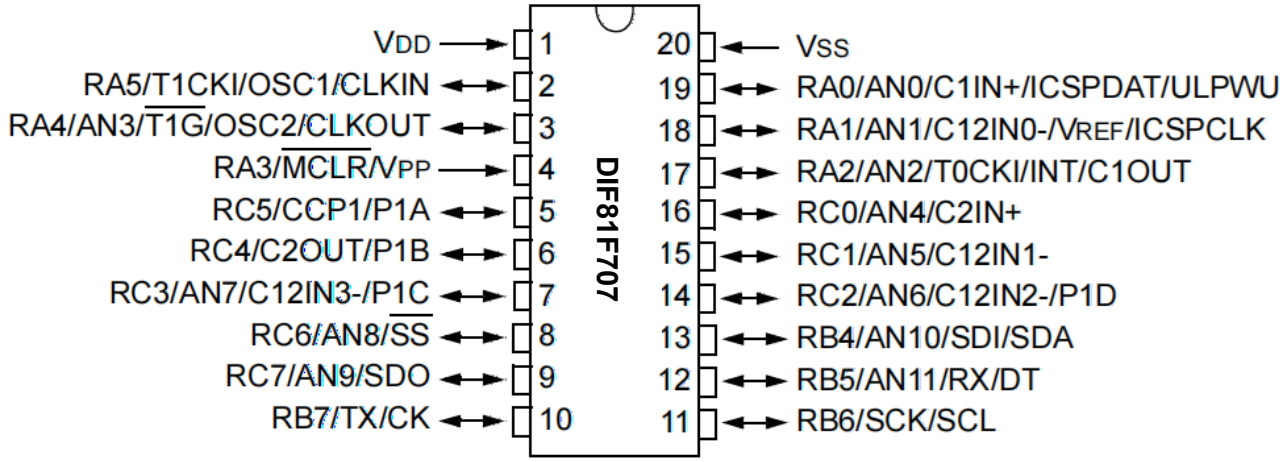
- 17 I/O Pins and 1 Input-Only Pin:
  - High current source/sink for direct LED drive
  - Interrupt-on-Change pin
  - Individually programmable weak pull-ups
  - Ultra Low-Power Wake-up (ULPWU)
- Analog Comparator Module with:
  - Two analog comparators
  - Programmable on-chip voltage reference(CVREF) module (% of VDD)
  - Comparator inputs and outputs externally accessible
  - SR Latch mode
  - Timer 1 Gate Sync Latch
  - Fixed 0.6V VREF
- A/D Converter:
  - 10-bit resolution and 12 channels
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

- Enhanced Capture, Compare, PWM+ Module:
- 16-bit Capture, max resolution 12.5 ns - Compare, max resolution 200 ns
- 10-bit PWM with 1, 2 or 4 output channels, programmable "dead time", max frequency 20 kHz
- PWM output steering control
- Synchronous Serial Port (SSP):
  - SPI mode (Master and Slave)
- I2C (Master/Slave modes):
  - I2C address mask
- In-Circuit Serial Programming (ICSP) via Two Pins

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit	SSP	ECCP+	EUSART
	Flash (words)	SRAM (bytes)	EEPROM (bytes)							
DIF81F707	4096	256	256	18	12	2	1/1	Yes	No	Yes

Pin Diagram

DIF81F707SI(20-pin SOP),
DIF81F707XI(20-pin SSOP)



DIF81F707 Pin Diagram

Table 1. DIF81F707 PIN SUMMARY

I/O	Pin	Analog	Comparators	Timers	EUSART	SSP	Interrupt	Pull-up	Basic
RA0	19	AN0/ULPWU	C1IN+	—	—	—	IOC	Y	ICSPDAT
RA1	18	AN1/VREF	C12IN0-	—	—	—	IOC	Y	ICSPCLK
RA2	17	AN2	C1OUT	T0CKI	—	—	IOC/INT	Y	
RA3	4	—	—	—	—	—	IOC	Y(1)	MCLR/VPP
RA4	3	AN3	—	T1G	—	—	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	T1CKI	—	—	IOC	Y	OSC1/CLKIN
RB4	13	AN10	—	—	—	SDI/SDA	IOC	Y	—
RB5	12	AN11	—	—	RX/DT	—	IOC	Y	—
RB6	11	—	—	—	—	SCL/SCK	IOC	Y	—
RB7	10	—	—	—	TX/CK	—	IOC	Y	—
RC0	16	AN4	C2IN+	—	—	—	—	—	—
RC1	15	AN5	C12IN1-	—	—	—	—	—	—
RC2	14	AN6	C12IN2-	—	—	—	—	—	—
RC3	7	AN7	C12IN3-	—	—	—	—	—	—
RC4	6	—	C2OUT	—	—	—	—	—	—
RC5	5	—	—	—	—	—	—	—	—
RC6	8	AN8	—	—	—	SS	—	—	—
RC7	9	AN9	—	—	—	SDO	—	—	—
—	1	—	—	—	—	—	—	—	VDD
—	20	—	—	—	—	—	—	—	VSS

CPU Kernel

Structural review

Figure 1 shows the block diagram of the DIF81F707device。

Table 1 shows the pin arrangement instructions.

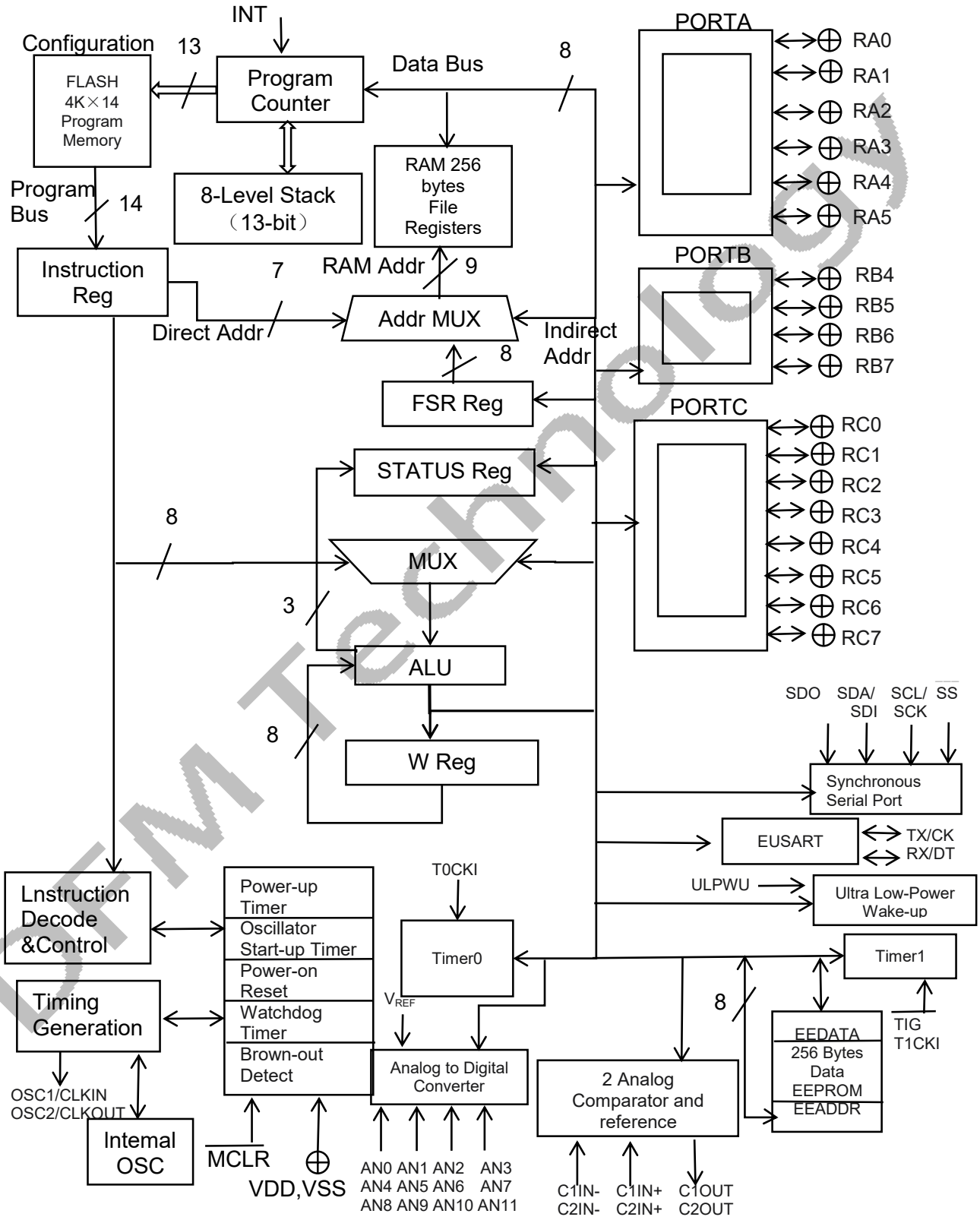


Figure 1. DIF81F707 BLOCK DIAGRAM

Table 2. PINOUT DESCRIPTION – DIF81F707

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT/ ULPWU	RA0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN0	AN	—	A/D Channel 0 input.
	C1IN+	AN	—	Comparator C1 positive input.
	ICSPDAT	TTL	CMOS	ICSP Data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/AN1/C12IN0-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN1	AN	—	A/D Channel 1 input.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF	AN	—	External Voltage Reference for A/D.
	ICSPCLK	ST	—	ICSP clock.
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN2	AN	—	A/D Channel 2 input.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External Interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
$\overline{\text{RA3}}$/MCLR/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
$\overline{\text{RA4}}$/AN3/T1G/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN3	AN	—	A/D Channel 3 input.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate input.
	OSC2	—	XTAL	Crystal/Resonator.
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	T1CKI	ST	—	Timer1 clock input.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	External clock input/RC oscillator connection.
RB4/AN10/SDI/SDA	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	SDI	ST	—	SPI data input.
	SDA	ST	OD	I^2C data input/output.
RB5/AN11/RX/DT	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.

Legend: AN = Analog input or output CMOS=CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels

HV = High Voltage XTAL= Crystal

Name	Function	Input Type	Output Type	Description
RB6/SCK/SCL	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	SCK	ST	CMOS	SPI clock.
	SCL	ST	OD	I^2C clock.
RB7/TX/CK	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on- change. Individually enabled pull-up.
	TX	—	CMOS	EUSART asynchronous output.
	CK	ST	CMOS	EUSART synchronous clock.
RC0/AN4/C2IN+	RC0	ST	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	C2IN+	AN	—	Comparator C2 positive input.
RC1/AN5/C12IN1-	RC1	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
RC2/AN6/C12IN2-	RC2	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
RC3/AN7/C12IN3-	RC3	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
RC4/C2OUT	RC4	ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
RC5	RC5	ST	CMOS	General purpose I/O.
$\overline{\text{RC6}}$/AN8/$\overline{\text{SS}}$	RC6	ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	$\overline{\text{SS}}$	ST	—	Slave Select input.
RC7/AN9/SDO	RC7	ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	SDO	—	CMOS	SPI data output.
V_{SS}	V_{SS}	Power	—	Ground reference.
V_{DD}	V_{DD}	Power	—	Positive supply.

Legend: AN = Analog input or output CMOS=CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HV = High Voltage XTAL= Crystal

MEMORY ORGANIZATION

Program Memory Organization

The DIF81F707 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 4K x 14 (0000h-0FFFh) for the DIF81F707. Accessing a location above these boundaries will cause a wraparound. The Reset vector is at 0000h and the interrupt vector is at 0004h.

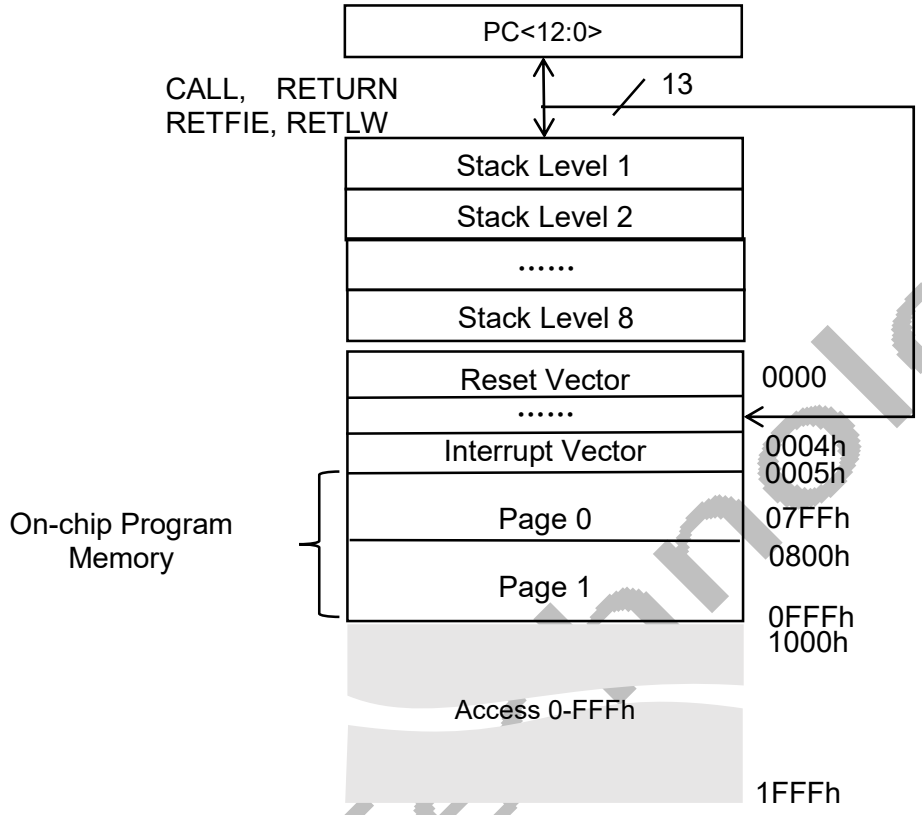


Figure 2. PROGRAM MEMORY MAP AND STACK FOR THE DIF81F707

Data Memory Organization

The data memory is partitioned into four banks which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. The General Purpose Registers, implemented as static RAM, are located in the last 96 locations of each Bank. Register locations F0h-FFh in Bank 1, 170h-17Fh in Bank 2 and 1F0h-1FFh in Bank 3 point to addresses 70h-7Fh in Bank 0. The actual number of General Purpose Resisters (GPR) in each Bank depends on the device. All other RAM is unimplemented and returns '0' when read. RP<1:0> of the STATUS register are the bank select bits:

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 in the DIF81F707. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) .

SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Registers related to the operation of peripheral features are described in the section of that peripheral feature.

	File Address		File Address		File Address		File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	PORTA	105h	TRISA	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	PORTC	107h	TRISC	187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDAT	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH(3)	10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH(3)	10Fh		18Fh
T1CON	10h	OSCTUNE	90h		110h		190h
	11h		91h		111h		191h
	12h		92h		112h		192h
SSPBUF	13h	SSPADD(2)	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
	15h	WPUA	95h	WPUB	115h		195h
	16h	IOCA	96h	IOCB	116h		196h
	17h	WDTCON	97h		117h		197h
RCSTA	18h	TXSTA	98h	VRCON	118h		198h
TXREG	19h	SPBRG	99h	CM1CON0	119h		199h
RCREG	1Ah	SPBRGH	9Ah	CM2CON0	11Ah		19Ah
	1Bh	BAUDCTL	9Bh	CM2CON1	11Bh		19Bh
	1Ch		9Ch		11Ch		19Ch
	1Dh		9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh	ANSEL	11Eh	SRCON	19Eh
ADCON0	1Fh	ADCON1	9Fh	ANSELH	11Fh		19Fh
General Purpose Register 96 Bytes	20h 7Fh	General Purpose Register 32 Bytes	A0h BFh	General Purpose Register 80 Bytes	120h		1A0h
		48 Bytes (PIC16F689 only)	C0h EFh	(PIC16F689 only)	170h 17Fh		
		accesses 70h-7Fh	F0h FFh	accesses 70h-7Fh		accesses 70h-7Fh	1F0h 1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

FIGURE 1.DIF81F707 SPECIAL FUNCTION REGISTERS

Table 3. DIF81F707 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
	Bank 0									
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx
06h	PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx-- -
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx
08h	—	Unimplemented								—
09h	—	Unimplemented								—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF (1)	0000 000x
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000
0Dh	PIR2	OSFIF	C2IF	C1IF	EEIF	—	—	—	—	0000----
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000
11h	TMR2	Timer2 Module Register								0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx
14h	SSPCON(2)	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx
17h	CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	
19h	TXREG	EUSART Transmit Data Register								
1Ah	RCREG	EUSART Transmit Data Register								
1Bh	—	Unimplemented								
1Ch	PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000
1Dh	ECCPAS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx
1Fh	ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: MCLR and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.

2: DIF81F707 only.

3: DIF81F707 only.

4: DIF81F707 only.

5: When SSPCON register bits SSPM<3:0> = 1001, any reads or writes to the SSPADD SFR address are accessed through the SSPMSK register. See Registers 13-2 and 13-3 for more detail.

6: Port pins with analog functions controlled by the ANSEL and ANSELH registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

Table 4. DIF81F707 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 1										
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81h	OPTION_REG	$\overline{RABPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111
88h	—	Unimplemented								—
89h	—	Unimplemented								—
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF(1)	0000 000x
8Ch	PIE1	—	ADIE(4)	RCIE(2)	TXIE(2)	SSPIE(5)	CCP1IE(3)	TMR2IE(3)	TMR1IE	-000 0000
8Dh	PIE2	OSFIE	C2IE	C1IE	EEIE	—	—	—	—	0000 ----
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$	--01 --qq
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000
91h	—	Unimplemented								—
92h	PR2(3)	Timer2 Period Register								1111 1111
93h	SSPADD(5, 7)	Synchronous Serial Port (I^2C mode) Address Register								0000 0000
93h	SSPMSK(5, 7)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	1111 1111
94h	SSPSTAT(5)	SMP	CKE	$\overline{D/A}$	P	S	$\overline{R/W}$	UA	BF	0000 0000
95h	WPUA(6)	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000
97h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000
98h	TXSTA(2)	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010
99h	SPBRG(2)	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000
9Ah	SPBRGH(2)	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	0000 0000
9Bh	BAUDCTL(2)	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00
9Ch	—	Unimplemented								—
9Dh	—	Unimplemented								—
9Eh	ADRESL(4)	A/D Result Register Low Byte								xxxx xxxx
9Fh	ADCON1(4)	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----

Legend: - = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: MCLR and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.

2: DIF81F707 only.

3: DIF81F707 only.

4: DIF81F707 only.

5: RA3 pull-up is enabled when pin is configured as MCLR in Configuration Word.

6: Accessible only when SSPCON register bits SSPM<3:0> = 1001.

Table5. DIF81F707 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 2										
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
101h	TMR0	Timer0 Module Register								xxxx xxxx
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
105h	PORTA(4)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx
106h	PORTB(4)	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----
107h	PORTC(4)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx
108h	—	Unimplemented								—
109h	—	Unimplemented								—
10Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF(1)	0000 000x
10Ch	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000
10Dh	EEADR	EEADR7(3)	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000
10Eh	EEDATH(2)	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000
10Fh	EEADRH(2)	—	—	—	—	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---- 0000
110h	—	Unimplemented								—
111h	—	Unimplemented								—
112h	—	Unimplemented								—
113h	—	Unimplemented								—
114h	—	Unimplemented								—
115h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	1111 ----
116h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	0000 ----
117h	—	Unimplemented								—
118h	VRCON	C1VREN	C2VREN	VRR	VP6EN	VR3	VR2	VR1	VR0	0000 0000
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10
11Ch	—	Unimplemented								—
11Dh	—	Unimplemented								—
11Eh	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3(3)	ANS2(3)	ANS1	ANS0	1111 1111
11Fh	ANSELH(3)	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111

Legend: - = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.

2: DIF81F707 only.

3: DIF81F707 only.

4: Port pins with analog functions controlled by the ANSEL and ANSELH registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

Table 6. DIF81F707 SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
Bank 3										
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
181h	OPTION_REG	$\overline{RABPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
184h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----
187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111
188h	—	Unimplemented								—
189h	—	Unimplemented								—
18Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF(1)	0000 000x
18Ch	EECON1	EEPGD(2)	—	—	—	WRERR	WREN	WR	RD	x--- x000
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----
18Eh	—	Unimplemented								—
18Fh	—	Unimplemented								—
190h	—	Unimplemented								—
191h	—	Unimplemented								—
192h	—	Unimplemented								—
193h	—	Unimplemented								—
194h	—	Unimplemented								—
195h	—	Unimplemented								—
196h	—	Unimplemented								—
197h	—	Unimplemented								—
198h	—	Unimplemented								—
199h	—	Unimplemented								—
19Ah	—	Unimplemented								—
19Bh	—	Unimplemented								—
19Ch	—	Unimplemented								—
19Dh	PSTRCON(2)	—	—	—	STRSYNC	STRD	STRC	STRB	STRA	---0 0001
19Eh	SRCON	SR1	SR0	C1SEN	C2REN	PULSS	PULSR	—	—	0000 00--
19Fh	—	Unimplemented								—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RABIF bit will be cleared upon Reset but will set again if the mismatch exists.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias.....-40°C to+125°C

Storage temperature.....-65°C to+150°C

Voltage on VDD with respect to VSS.....-0.3to+6.5V

Voltage on MCLR with respect to Vss.....-0.3to +13.5V

Voltage on all other pins with respect to VSS.....-0.3V to (VDD + 0.3V)

Total power dissipation(1).....800mW

Maximum current out of VSS pin.....300 mA

Maximum current into VDD pin.....250 mA

Input clamp current, IIK (VI < 0 or VI > VDD).....±20 mA

Output clamp current, IOK (Vo < 0 or Vo >VDD).....±20 mA

Maximum output current sunk by any I/O pin.....25 mA

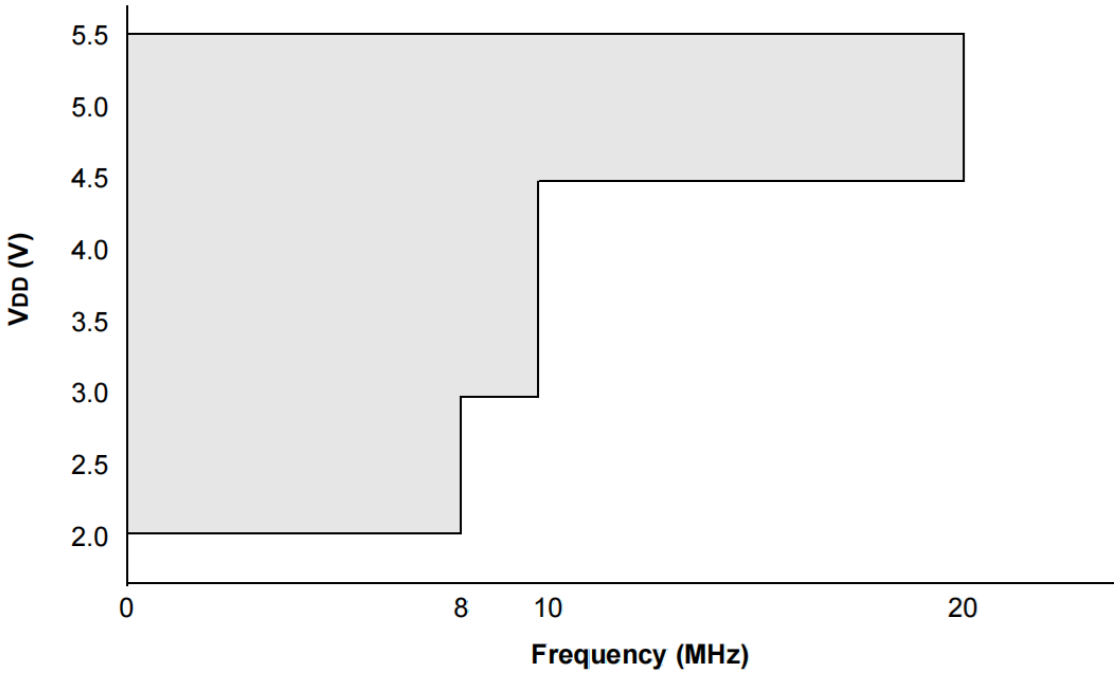
Maximum output current sourced by any I/O pin.....25 mA

Maximum current sunk by PORTA, PORTB and PORTC 200mA

Maximum current sourced PORTA, PORTB and PORTC 200mA

Note1：Power dissipation is calculated as follows: $P_{DIS} = V_{DD} * \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL}*I_{OL})$.

Note： Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 ohm should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to VSS.



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 4.DIF81F707 VOLTAGE-FREQUENCY GRAPH， -40°C ≤ TA ≤ +125°C

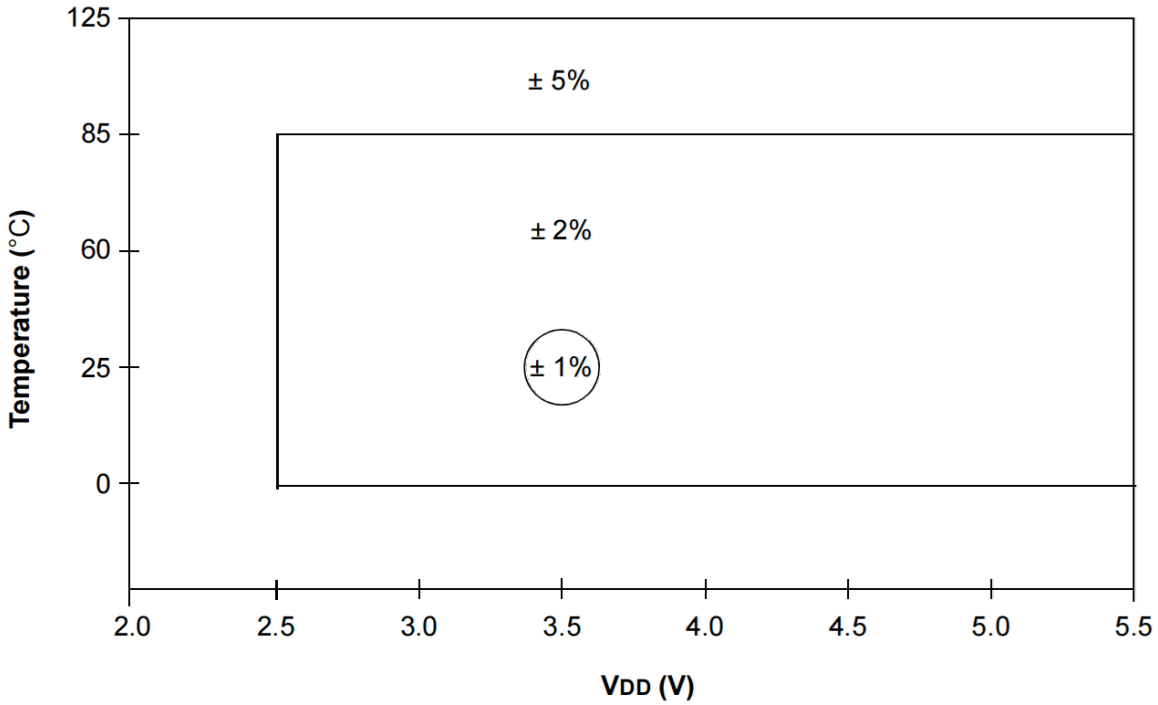


FIGURE 5. HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

DC Characteristics: DIF81F707

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C TA +85°C for industrial -40°C □ TA □ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Type	Max.	Units	Conditions
D001 D001C D001D	VDD	Supply Voltage	2.0 2.0 3.0 4.5	— — — —	5.5 5.5 5.5 5.5	V V V V	FOSC<=8MHz：HFINTOSC, EC FOSC < = 4 MHz FOSC < = 10 MHz FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage**(1)	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	_
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	_

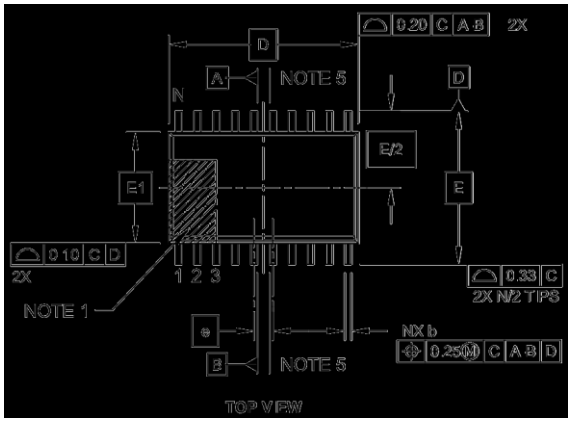
* These parameters are characterized but not tested.

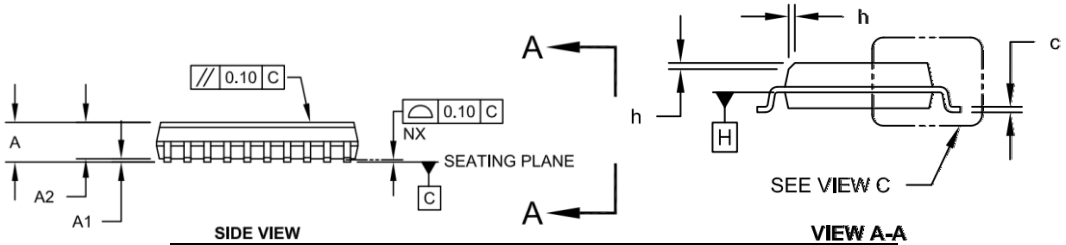
† Data in "Type" column is at 5.0V, 25° C unless otherwise stated. These parameters are for design guidance only and are not tested.

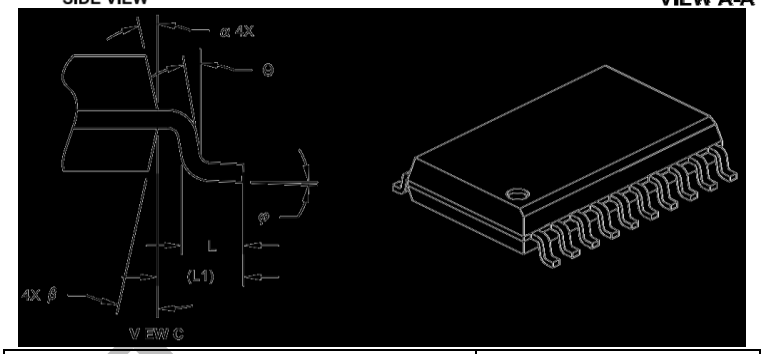
Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

Package Details

DIF81F707SI, 20-Lead Plastic Small Outline (SO)-Wide, 7.50 mm Body [SOIC]





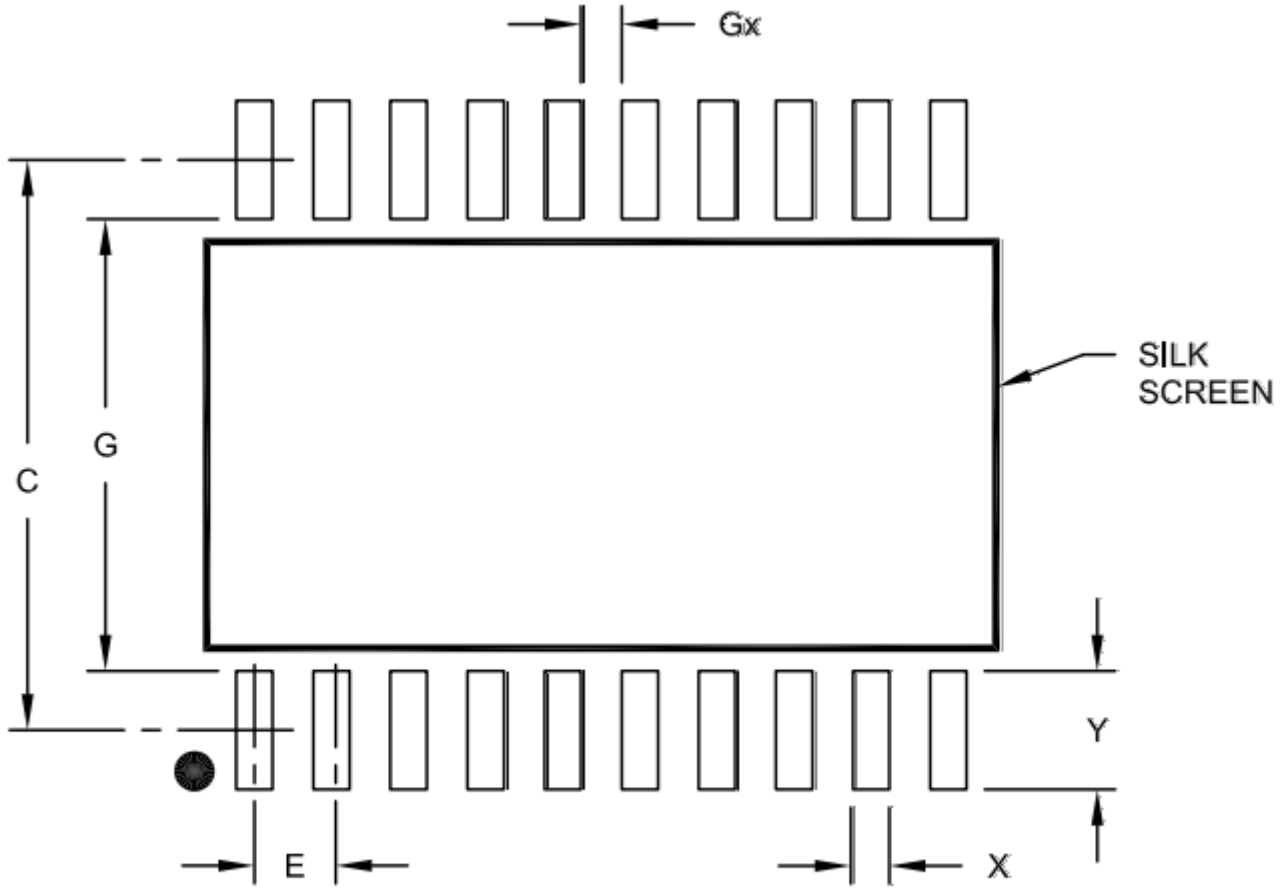


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.1.27 BSC	
Over Height	A	—	—	2.65
Molded Package Thickness	A2	2.05	—	—
Standoff §	A1	0.10	—	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer(Optional)	h	0.25	—	0.75
Foot Length	L	0.40	—	1.27
Footprint	L1		1.40 REF	
Foot Angle	ϕ	0°	—	8°
Lead Thickness	c	0.20	—	0.33
Lead Width	b	0.31	—	0.51
Mold Draft Angle Top	α	5°	—	15°
Mold Draft Angle Bottom	β	5°	—	15°

Notes：

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not induce mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end.
   Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and telebanking per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datum’s A & B to be determined at Datum H.

DIF81F707SI, 20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]



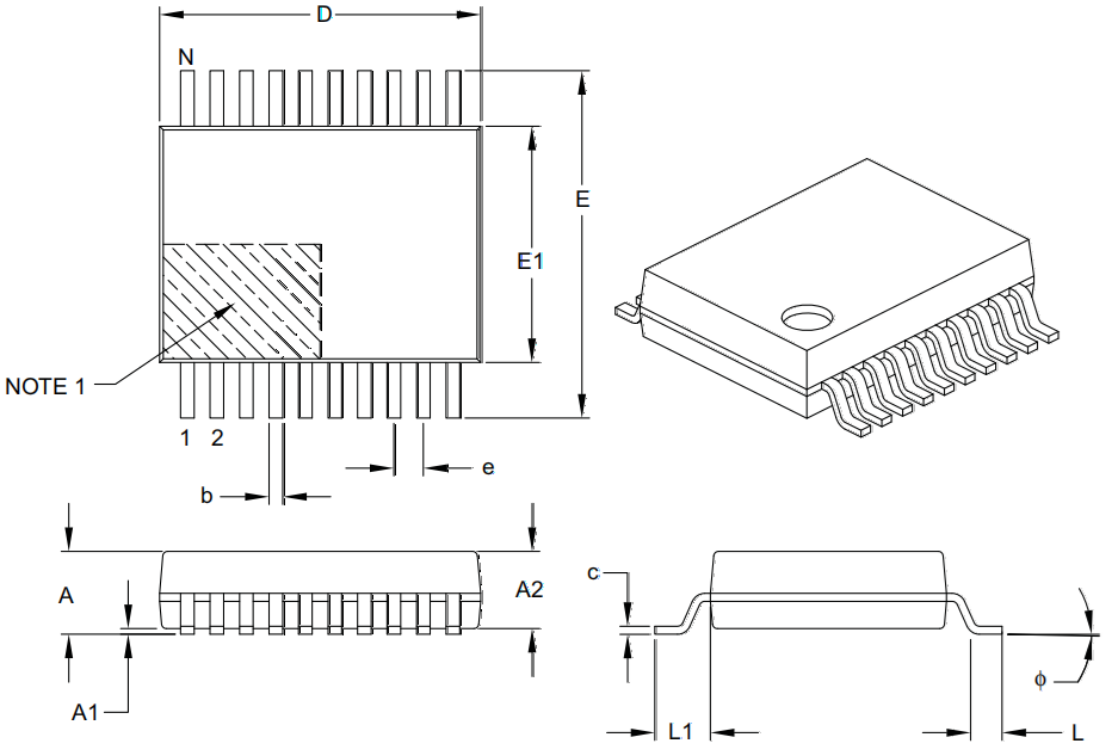
RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width(X20)	X			0.60
Contact Pad Length(X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F707XI, 20-Lead Plastic Shrink Small Outline (ss)- 5.30 mm Body [SSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Over Height	A	—	—	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	—	—
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Foot Angle	ϕ	0°	4°	8°
Lead Thickness	c	0.09	—	0.25
Lead Width	b	0.22	—	0.38

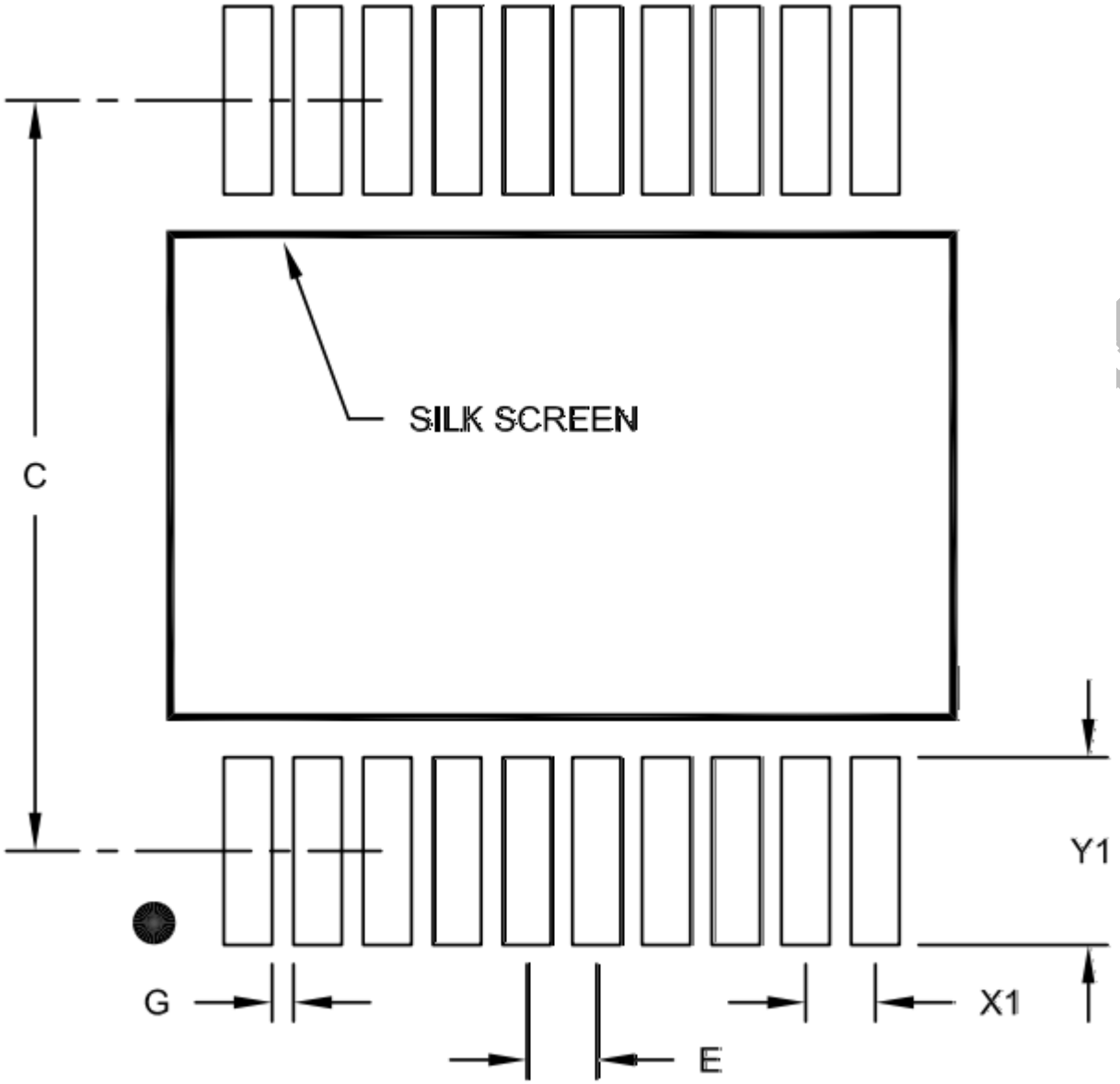
Notes：

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F707XI, 20-Lead Plastic Shrink Small Outline (ss)- 5.30 mm Body [SSOP]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width(X20)	X			0.45
Contact Pad Length(X20)	Y			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.