Difmicro Technolog

DIF81F666

Datasheet

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DIF81F666 Product characteristics

High-Performance RISC CPU:

- Operating speeds from DC – 20 MHz
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes
- 35 single-word instructions:
  - All instructions single cycle except branches

Special Microcontroller Features:

- Internal and external oscillator options:
  - Precision internal 4 MHz oscillator factory calibrated to ±1%
  - Low-power internal 48 kHz oscillator
  - External Oscillator support for crystals and resonators
- Power-saving Sleep mode
- Programmable weak pull-ups on PORTB
- Multiplexed Master Clear/Input-pin
- Watchdog Timer with independent oscillator for reliable operation
- Low-voltage programming
- In-Circuit Serial Programming (via two pins)
- Programmable code protection
- Brown-out Reset
- Power-on Reset
- Power-up Timer and Oscillator Start-up Timer
- Wide operating voltage range (2.0-5.5V)
- Industrial and extended temperature range
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - 40 years data retention

Low-Power Features:

- Standby Current:
  - 100 nA @ 2.0V, typical
- Operating Current:
  - 12 μA @ 32 kHz, 2.0V, typical
  - 120 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical
- Timer1 Oscillator Current:
  - 1.2 μA @ 32 kHz, 2.0V, typical
- Dual-speed Internal Oscillator:
  - Run-time selectable between 4 MHz and 48 kHz
  - 4 μs wake-up from Sleep, 3.0V, typical

Peripheral Features:

- 16 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Timer1: 16-bit timer/counter with external crystal/ clock capability
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture/Compare
  - 10-bit PWM
- Addressable Universal Synchronous/Asynchronous Receiver/Transmitter USART/SCI

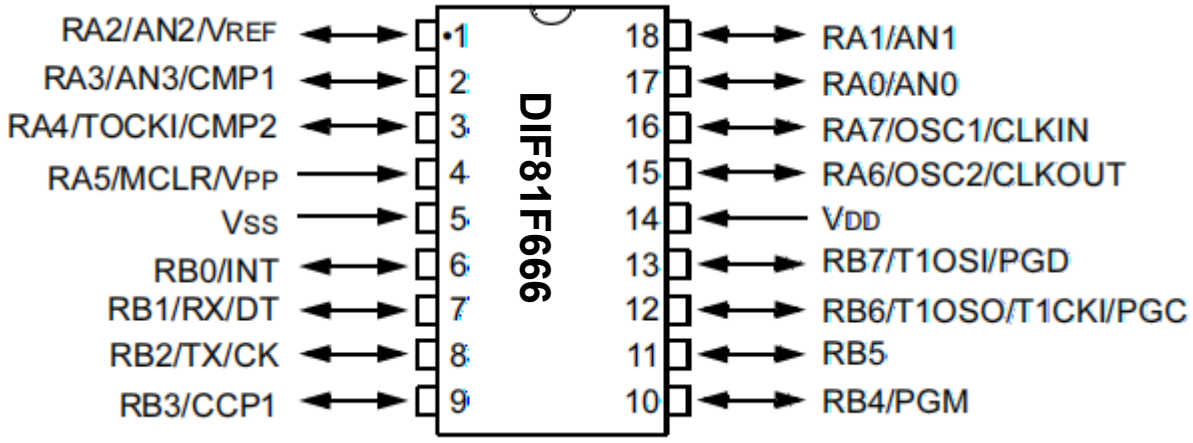
Table 1.DIF81F666

Device	Program Memory	Data Memory		I/O	CCP (PWM)	USART	Comparators	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)					
DIF81F666	4096	256	256	16	1	Y	2	2/1

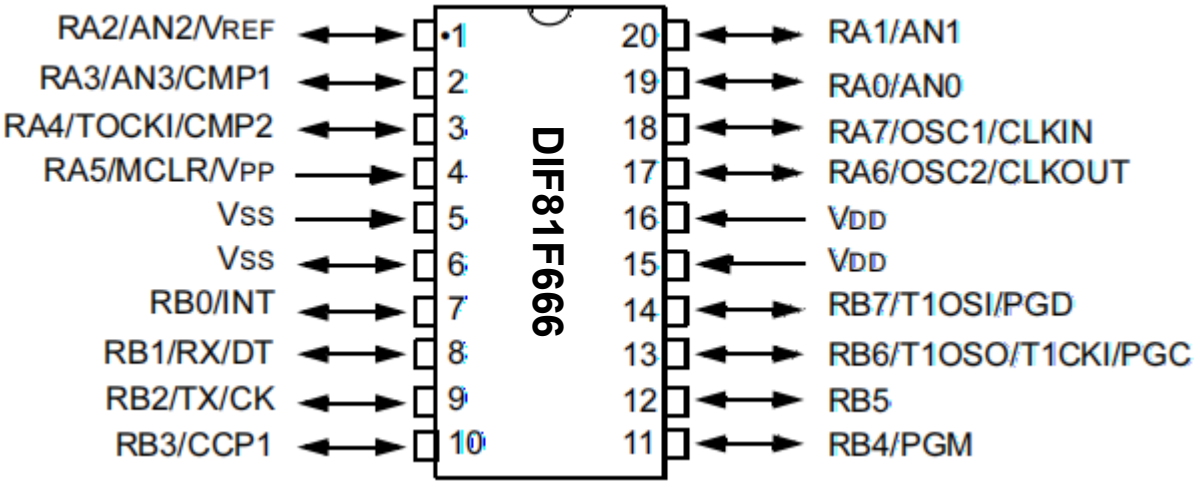
Pin Diagrams

DIF81F666DI(18-pin DIP)

DIF81F666SI(18-pin SOP)



DIF81F666XI(20-pin SSOP)



CPU Kernel

DEVICE OVERVIEW

The high performance of the DIF81F666 family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the DIF81F666 uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional Von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single-word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The Table below lists program memory (FLASH, Data and EEPROM).

Table 2.DIF81F666 MEMORY

Device	Memory		
	FLASH Program	RAM Data	EEPROM Data
DIF81F666	4096 x 14	256 x 8	256 x 8

The DIF81F666 can directly or indirectly address its register files or data memory. All Special Function Registers (SFR), including the program counter, are mapped in the data memory. The DIF81F666 have an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of 'special optimal situations' makes programming with the DIF81F666 simple yet efficient. In addition, the learning curve is reduced significantly.

The DIF81F666 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the Status Register. The C and DC bits operate as Borrow and Digit Borrow out bits, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in **Figure *1***, and a description of the device pins in **Table *3***.

Two types of data memory are provided on the DIF81F666 devices. Nonvolatile EEPROM data memory is provided for long term storage of data, such as calibration values, look-up table data, and any other data which may require periodic updating in the field. These data types are not lost when power is removed. The other data memory provided is regular RAM data memory. Regular RAM data memory is provided for temporary storage of data during normal operation. Data is lost when power is removed.

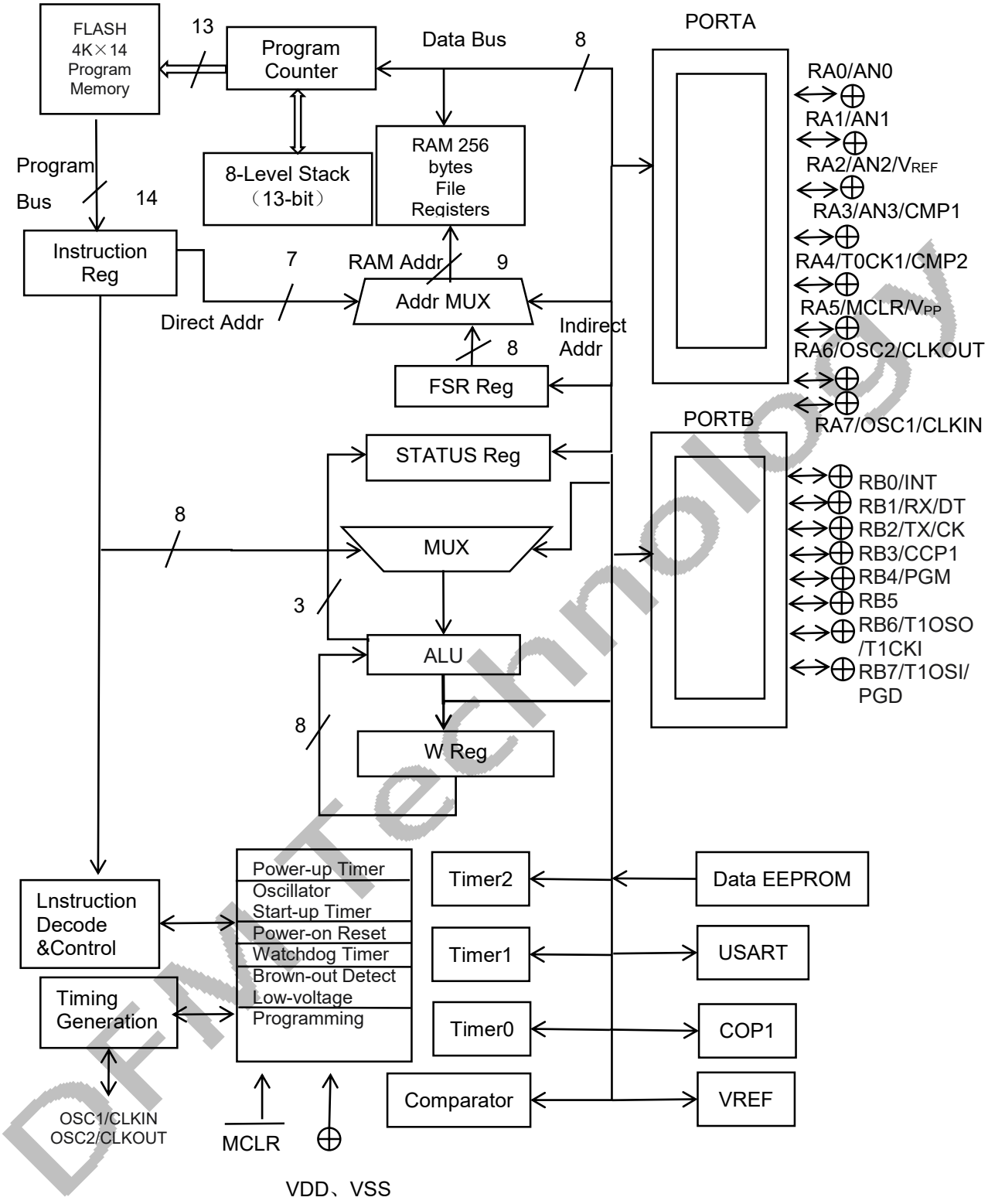


Figure 1. BLOCK DIAGRAM

Note 1: Higher order bits are from the STATUS register.

Table 3. DIF81F666 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	ST	CMOS	Bi-directional I/O port
	AN0	AN	—	Analog comparator input
RA1/AN1	RA1	ST	CMOS	Bi-directional I/O port
	AN1	AN	—	Analog comparator input
RA2/AN2/VREF	RA2	ST	CMOS	Bi-directional I/O port
	AN2	AN	—	Analog comparator input
	VREF	—	AN	VREF output
RA3/AN3/CMP1	RA3	ST	CMOS	Bi-directional I/O port
	AN3	AN	—	Analog comparator input
	CMP1	—	CMOS	Comparator 1 output
RA4/T0CKI/CMP2	RA4	ST	OD	Bi-directional I/O port
	T0CKI	ST	—	Timer0 clock input
	CMP2	—	OD	Comparator 2 output
RA5/$\overline{\text{MCLR}}$/VPP	RA5	ST	—	Input port
	$\overline{\text{MCLR}}$	ST	—	Master clear
	VPP	—	—	Programming voltage input. When configured as MCLR, this pin is an active low RESET to the device. Voltage on MCLR/VPP must not exceed VDD during normal device operation.
RA6/OSC2/CLKOUT	RA6	ST	CMOS	Bi-directional I/O port
	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In ER/INTRC mode, OSC2 pin can output CLKOUT, which has 1/4 the frequency of OSC1
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O port
	OSC1	XTAL	—	Oscillator crystal input
	CLKIN	ST	—	External clock source input. ER biasing pin.
RB0/INT	RB0	TTL	CMOS	Bi-directional I/O port. Can be software programmed for internal weak pull-up.
	INT	ST	—	External interrupt.
RB1/RX/DT	RB1	TTL	CMOS	Bi-directional I/O port. Can be software programmed for internal weak pull-up.
	RX	ST	—	USART receive pin
	DT	ST	CMOS	Synchronous data I/O.
RB2/TX/CK	RB2	TTL	CMOS	Bi-directional I/O port.
	TX	—	CMOS	USART transmit pin
	CK	ST	CMOS	Synchronous clock I/O. Can be software programmed for internal weak pull-up.
RB3/CCP1	RB3	TTL	CMOS	Bi-directional I/O port. Can be software programmed for internal weak pull-up.
	CCP1	ST	CMOS	Capture/Compare/PWM I/O

Legend: O = Output CMOS = CMOS Output P = Power,
— = Not used I = Input ST = Schmitt Trigger input
TTL = TTL input OD = Open Drain Output AN = Analog

Name	Function	Input Type	Output Type	Description
RB4/PGM	RB4	TTL	CMOS	Bi-directional I/O port. Can be software programmed for internal weak pull-up.
	PGM	ST	—	Low voltage programming input pin. Interrupt- on-pin change. When low voltage program- ming is enabled, the interrupt-on-pin change and weak pull-up resistor are disabled.
RB5	RB5	TTL	CMOS	Bi-directional I/O port. Interrupt-on-pin change. Can be software programmed for internal weak pull-up.
RB6/T1OSO/T1CKI/PGC	RB6	TTL	CMOS	Bi-directional I/O port. Interrupt-on-pin change. Can be software programmed for internal weak pull-up.
	T1OSO	—	XTAL	Timer1 oscillator output.
	T1CKI	ST	—	Timer1 clock input.
	PGC	ST	—	ICSP Programming Clock.
RB7/T1OSI/PGD	RB7	TTL	CMOS	Bi-directional I/O port. Interrupt-on-pin change. Can be software programmed for internal weak pull-up.
	T1OSI	XTAL	—	Timer1 oscillator input. Wake-up from SLEEP on pin change. Can be software programmed for internal weak pull-up.
	PGD	ST	CMOS	ICSP Data I/O
VSS	VSS	Power	—	Ground reference for logic and I/O pins
VDD	VDD	Power	—	Positive supply for logic and I/O pins

Legend: O = Output CMOS = CMOS Output P = Power,
— = Not used I = Input ST = Schmitt Trigger input
TTL = TTL input OD = Open Drain Output AN = Analog

Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN/RA7 pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4.

Instruction Flow/Pipelining

An “Instruction Cycle” consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change, (e.g., GOTO) then two cycles are required to complete the instruction.

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the “Instruction Register (IR)” in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

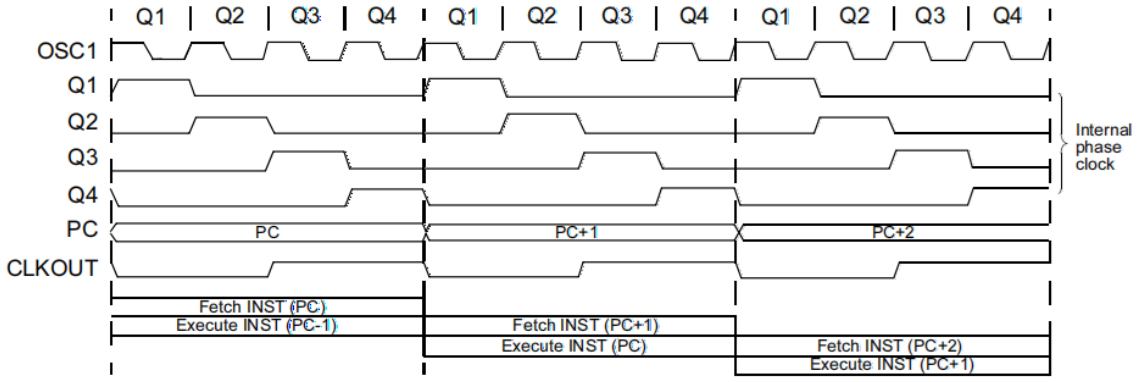


Figure 2.CLOCK/INSTRUCTION CYCLE

EXAMPLE:

```
1.CLRF    02h
2.CLRW
3.CLRF    GPIO
4.BSF     GPIO,BIT1
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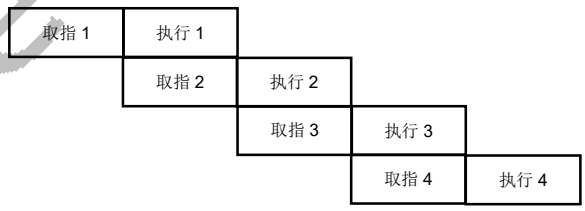


除程序转移指令外，所有指令都是单周期指令。由于程序转移指令将导致一条已取指令从流水线清除，需要重新取指，然后执行指令，所以程序转移指令需要两个周期。

MEMORY ORGANIZATION

Program Memory Organization for the DIF81F666

The DIF81F666 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 4K x 14 (0000h-0FFFh) for the DIF81F666 is physically implemented. Accessing a location above these boundaries will cause a wrap- around within the first 4K x 14 space (DIF81F666). The Reset vector is at 0000h and the interrupt vector is at 0004h.

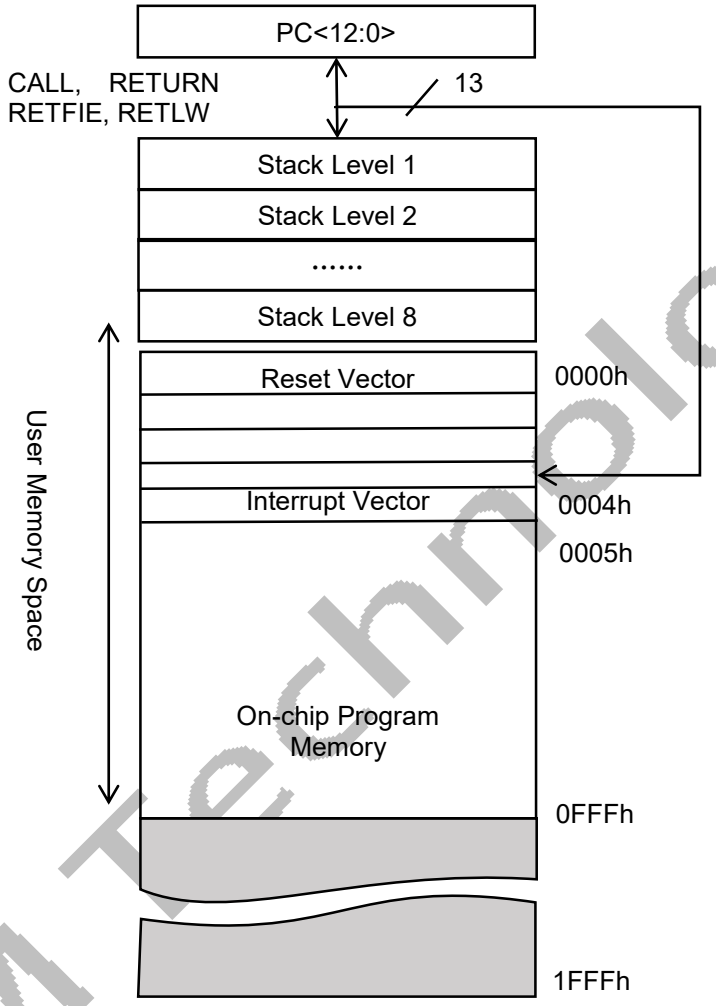


Figure 3.PROGRAM MEMORY MAP AND STACK

Data Memory Organization

The data memory is partitioned into four banks, which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). The SFRs are located in the first 32 locations of each bank. There are General Purpose Registers implemented as static RAM in each bank. **Table *4*** lists the General Purpose Register available in each of the four banks.

Table 4.GENERAL PURPOSE STATIC RAM REGISTERS

	DIF81F666
Bank0	20-7Fh
Bank1	A0h-FF
Bank2	120h-17Fh
Bank3	1F0h-1FFh

Addresses F0h-FFh, 170h-17Fh and 1F0h-1FFh are implemented as common RAM and mapped back to addresses 70h-7Fh.

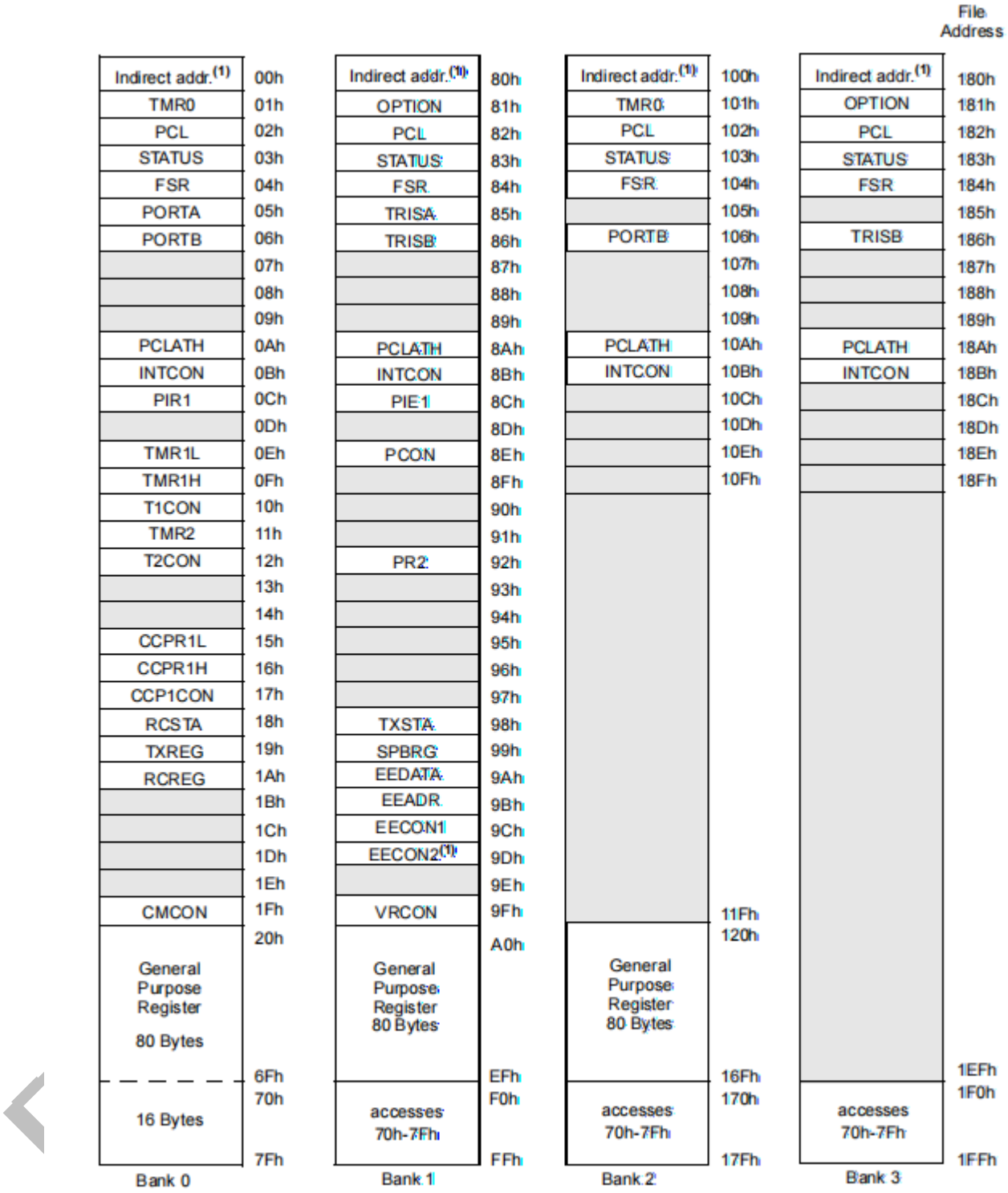
Table *5* lists how to access the four banks of registers via the Status register bits RP1 and RP0.

Table 5.ACCESS TO BANKS OF REGISTERS

Bank	RP1	RP0
0	0	0
1	0	1
2	1	0
3	1	1

GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 in the DIF81F666.Each is accessed either directly or indirectly through the File Select Register (FSR),



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

Figure 4.DATA MEMORY MAP OF THE DIF81F666

SPECIAL FUNCTION REGISTERS

The SFRs are registers used by the CPU and Peripheral functions for controlling the desired operation of the device **Table *6***. These registers are static RAM.

The special registers can be classified into two sets (core and peripheral). The SFRs associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

Table 6.SPECIAL REGISTERS SUMMARY BANK 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset(1)
Bank 0										
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module’s Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
04h	FSR	Indirect data memory address pointer								xxxx xxxx
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx
07h	—	Unimplemented								—
08h	—	Unimplemented								—
09h	—	Unimplemented								—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
0Ch	PIR1	EEIF	CMIF	RCIF	TXIF	—	CCP1IF	TMR2IF	TMR1IF	0000 -000
0Dh	—	Unimplemented								—
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000
11h	TMR2	TMR2 module's register								0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000
13h	—	Unimplemented								—
14h	—	Unimplemented								—
15h	CCPR1L	Capture/Compare/PWM register (LSB)								xxxx xxxx
16h	CCPR1H	Capture/Compare/PWM register (MSB)								xxxx xxxx
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADEN	FERR	OERR	RX9D	0000 -00x
19h	TXREG	USART Transmit data register								0000 0000
1Ah	RCREG	USART Receive data register								0000 0000
1Bh	—	Unimplemented								—
1Ch	—	Unimplemented								—
1Dh	—	Unimplemented								—
1Eh	—	Unimplemented								—
1Fh	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000

Legend: – = Unimplemented locations read as ‘0’, u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: For the Initialization Condition for Registers Tables

Table 7.SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset(1)
Bank 1										
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
84h	FSR	Indirect data memory address pointer								xxxx xxxx
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
87h	—	Unimplemented								—
88h	—	Unimplemented								—
89h	—	Unimplemented								—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
8Ch	PIE1	EEIE	CMIE	RCIE	TXIE	—	CCP1IE	TMR2IE	TMR1IE	0000 -000
8Dh	—	Unimplemented								—
8Eh	PCON	—	—	—	—	OSCF	—	$\overline{POR}$	$\overline{BOD}$	---- 1-0x
8Fh	—	Unimplemented								—
90h	—	Unimplemented								—
91h	—	Unimplemented								—
92h	PR2	Timer2 Period Register								1111 1111
93h	—	Unimplemented								—
94h	—	Unimplemented								—
95h	—	Unimplemented								—
96h	—	Unimplemented								—
97h	—	Unimplemented								—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000
9Ah	EEDATA	EEPROM data register								xxxx xxxx
9Bh	EEADR	—	EEPROM address register							xxxx xxxx
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000
9Dh	EECON2	EEPROM control register 2 (not a physical register)								--------
9Eh	—	Unimplemented								—
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: For the Initi**alization Condition** for Registers Tables

Table 8.SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset(1)
Bank 2										
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
101h	TMR0	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx
104h	FSR	Indirect data memory address pointer								xxxx xxxx
105h	—	Unimplemented								—
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx
107h	—	Unimplemented								—
108h	—	Unimplemented								—
109h	—	Unimplemented								—
10Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
10Ch	—	Unimplemented								—
10Dh	—	Unimplemented								—
10Eh	—	Unimplemented								—
10Fh	—	Unimplemented								—
110h	—	Unimplemented								—
111h	—	Unimplemented								—
112h	—	Unimplemented								—
113h	—	Unimplemented								—
114h	—	Unimplemented								—
115h	—	Unimplemented								—
116h	—	Unimplemented								—
117h	—	Unimplemented								—
118h	—	Unimplemented								—
119h	—	Unimplemented								—
11Ah	—	Unimplemented								—
11Bh	—	Unimplemented								—
11Ch	—	Unimplemented								—
11Dh	—	Unimplemented								—
11Eh	—	Unimplemented								—
11Fh	—	Unimplemented								—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: For the Initialization Condition for Registers Tables

Table 9.SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset(1)
Bank 3										
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
184h	FSR	Indirect data memory address pointer								xxxx xxxx
185h	—	Unimplemented								—
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
187h	—	Unimplemented								—
188h	—	Unimplemented								—
189h	—	Unimplemented								—
18Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
18Ch	—	Unimplemented								—
18Dh	—	Unimplemented								—
18Eh	—	Unimplemented								—
18Fh	—	Unimplemented								—
190h	—	Unimplemented								—
191h	—	Unimplemented								—
192h	—	Unimplemented								—
193h	—	Unimplemented								—
194h	—	Unimplemented								—
195h	—	Unimplemented								—
196h	—	Unimplemented								—
197h	—	Unimplemented								—
198h	—	Unimplemented								—
199h	—	Unimplemented								—
19Ah	—	Unimplemented								—
19Bh	—	Unimplemented								—
19Ch	—	Unimplemented								—
19Dh	—	Unimplemented								—
19Eh	—	Unimplemented								—
19Fh	—	Unimplemented								—

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias..... -40°C to +125°C
Storage temperature..... -65°C to +150°C
Voltage on VDD with respect to VSS.....-0.3 to +6.5V
Voltage on MCLR with respect to VSS.....-0.3 to +14V
Voltage on all other pins with respect to VSS.....-0.3V to (VDD + 0.3V)
Total power dissipation(1).....800 mW
Max. current out of VSS pin.....300 mA
Max. current into VDD pin.....250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > VDD).....±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > VDD).....±20 mA
Max. output current sunk by any I/O pin.....25 mA
Max. output current sourced by any I/O pin.....25 mA
Max. output current sourced by I/O port.....200 mA
Max. output current sunk by I/O port.....200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

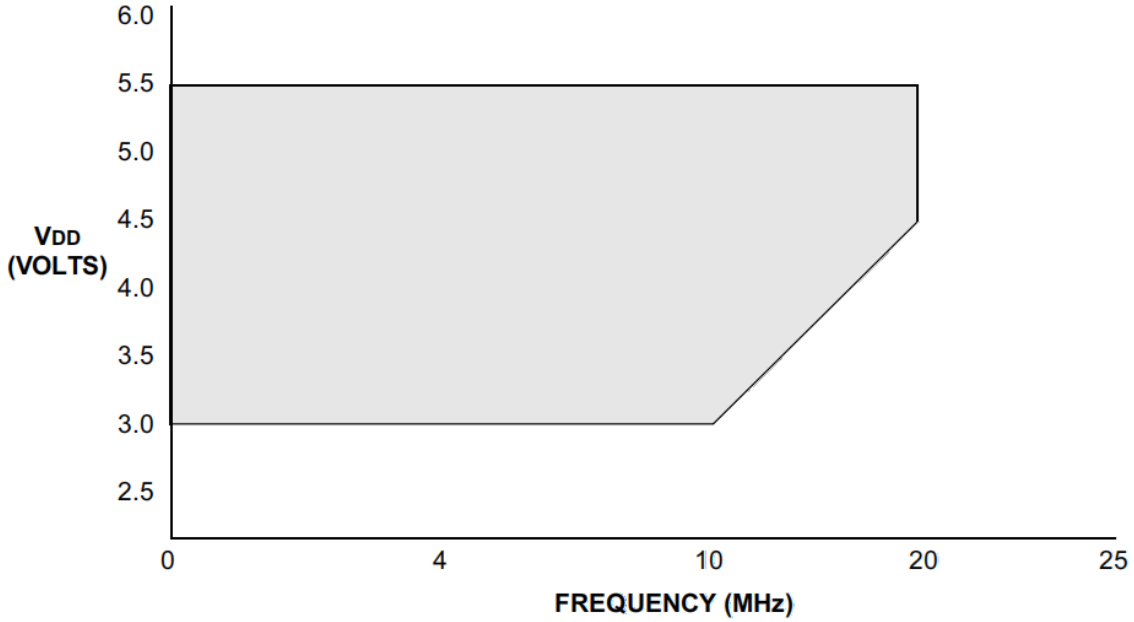


Figure 5.DIF81F666 VOLTAGE-FREQUENCY GRAPH,0℃≤ TA≤+70℃

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

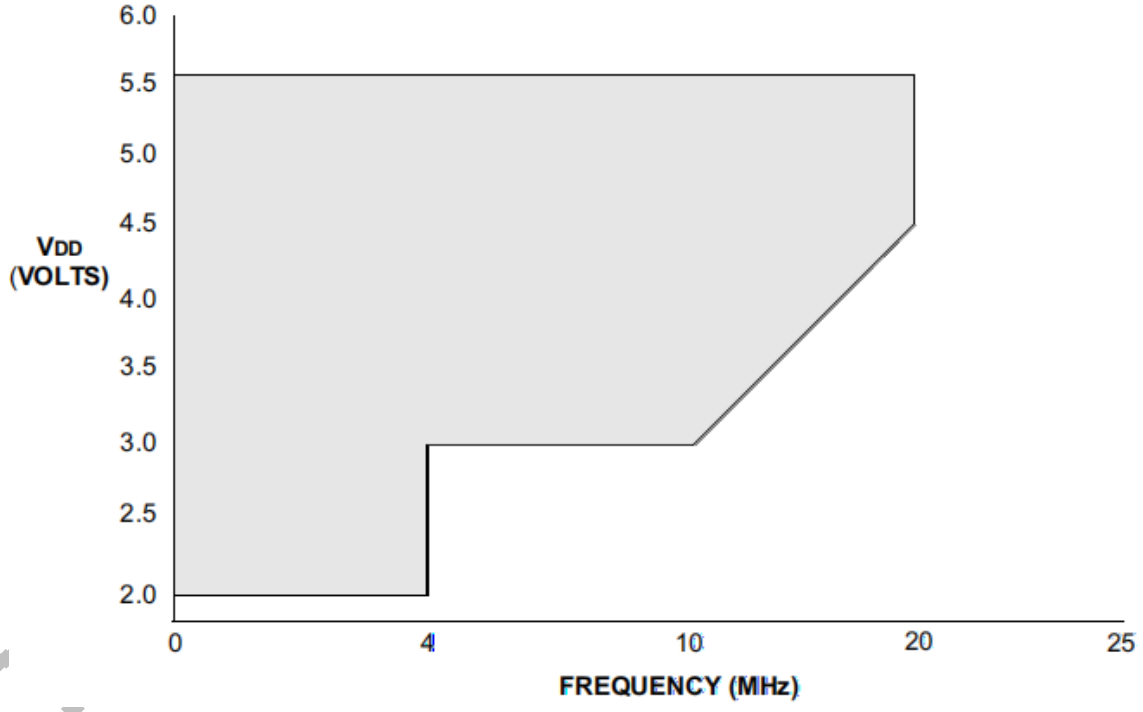


Figure 6.DIF81F666 VOLTAGE-FREQUENCY GRAPH,0℃≤ TA≤+70℃

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

DC Characteristics:DIF81F666

DIF81F666			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ Ta ≤ +85°C for industrial and 0°C ≤ Ta ≤ +70°C for commercial and -40°C ≤ Ta ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage					
D001		DIF81F666	3.0	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	Device in SLEEP mode*
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05	—	—	V/ms	
D005	VBOD	**Brown-out Detect Voltage**	3.65 3.65	4.0 —	4.35 4.4	V V	BODEN configuration bit is set BODEN configuration bit is set, Extended

Legend: Rows with standard voltage device data only are shaded for improved readability.

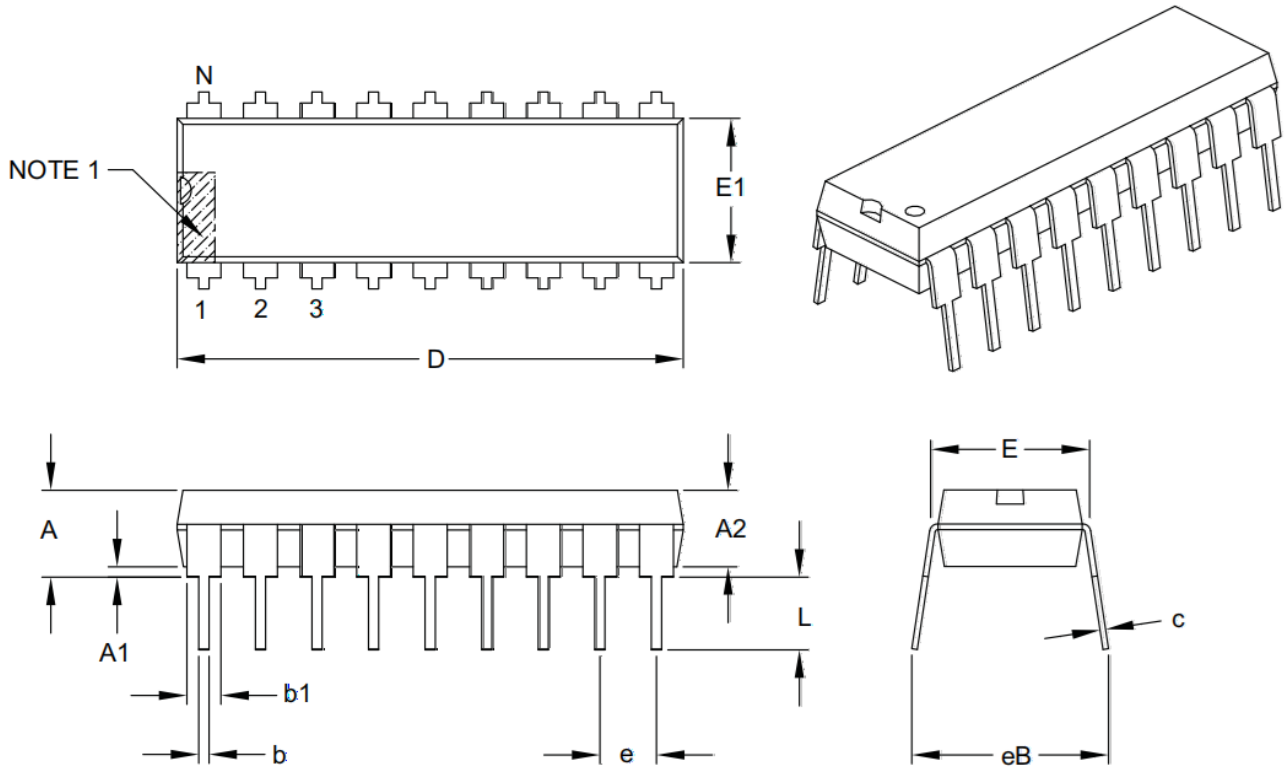
* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25° C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Package Details

DIF81F666DI, 18-Lead Plastic Dual In-line (P)-300 mil[DIP]



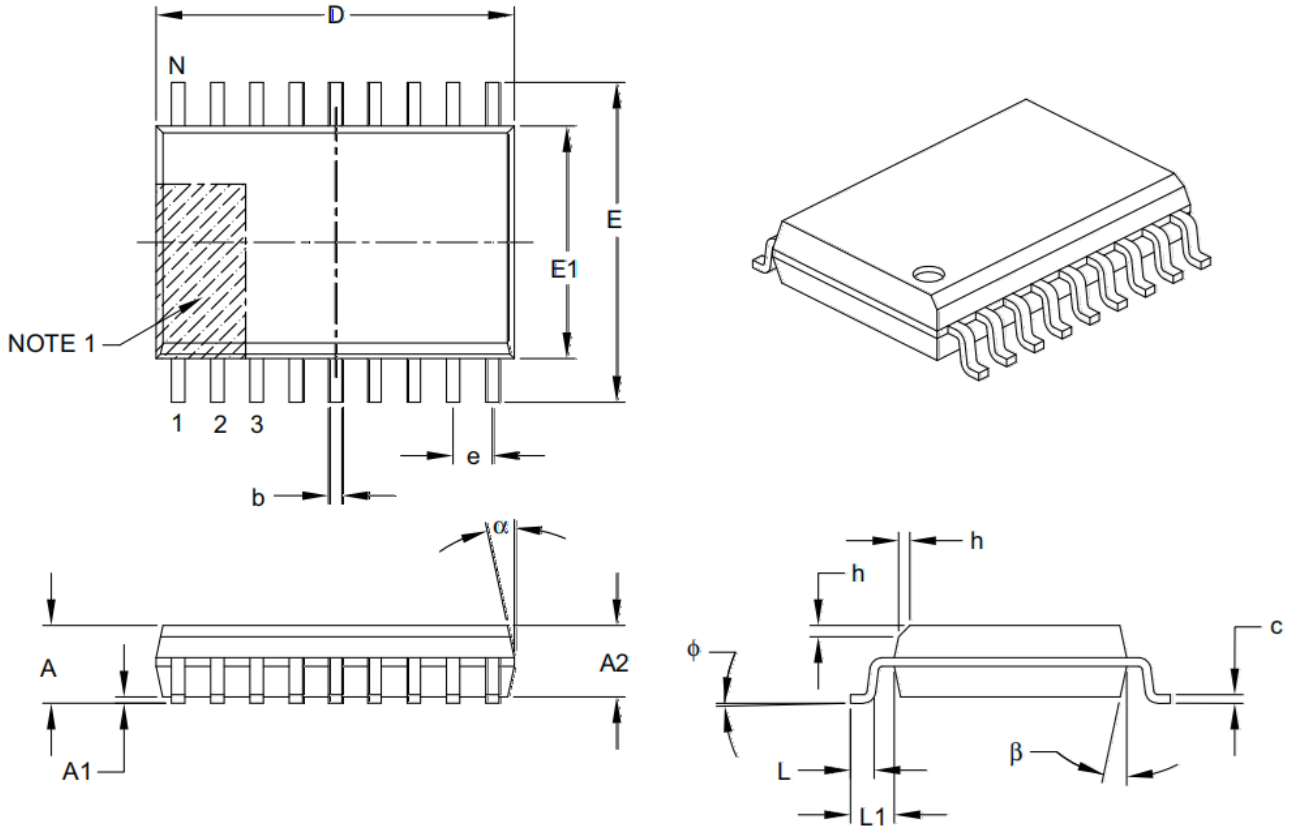
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F666SI, 18-Lead Plastic Small Outline (SO) -Wide, 300 mil[SOIC]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		11.55 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle		0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top		5°	–	15°
Mold Draft Angle Bottom		5°	–	15°

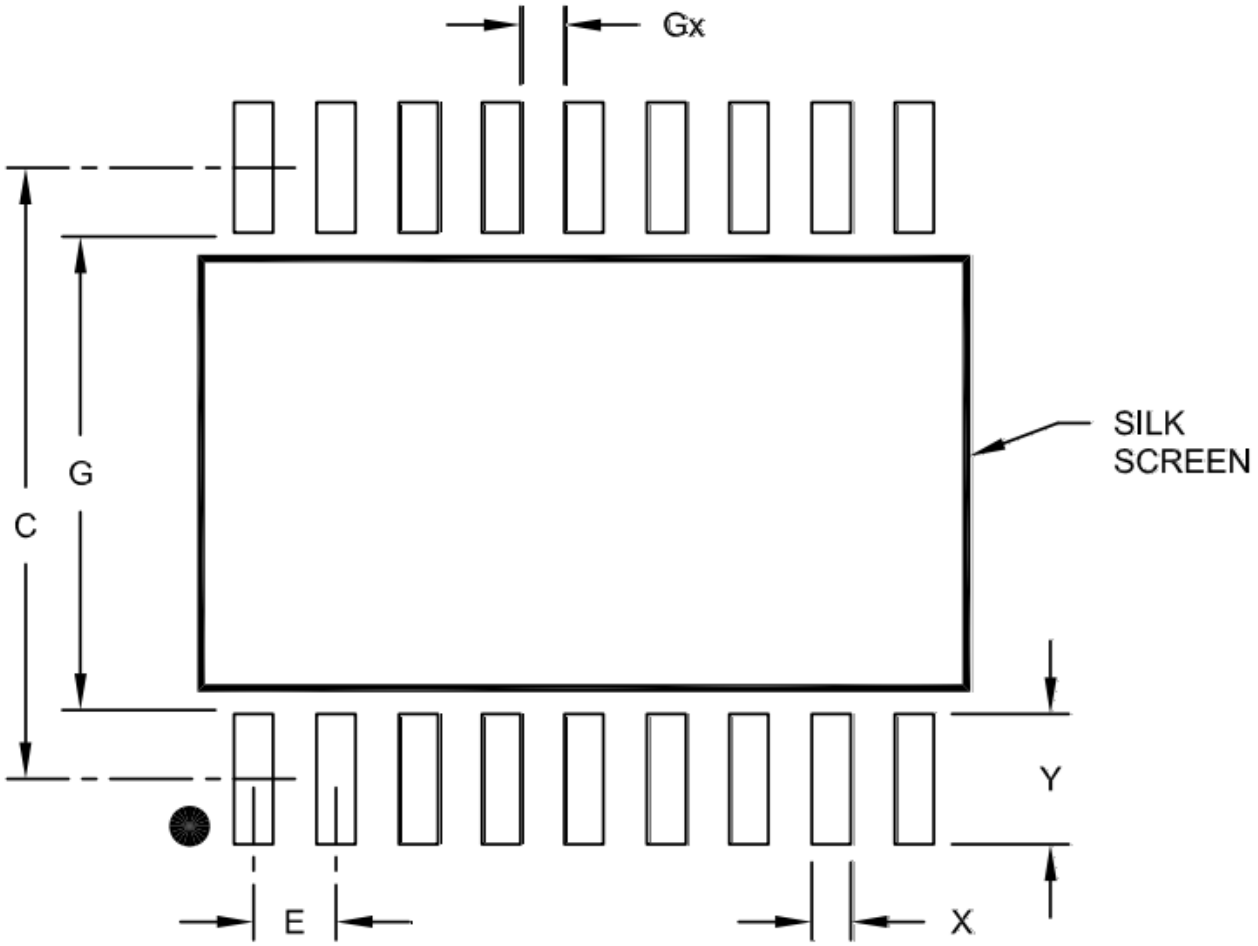
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F666SI, 18-Lead Plastic Small Outline (SO) -Wide, 300 mil[SOIC]



RECOMMENDED LAND PATTERN

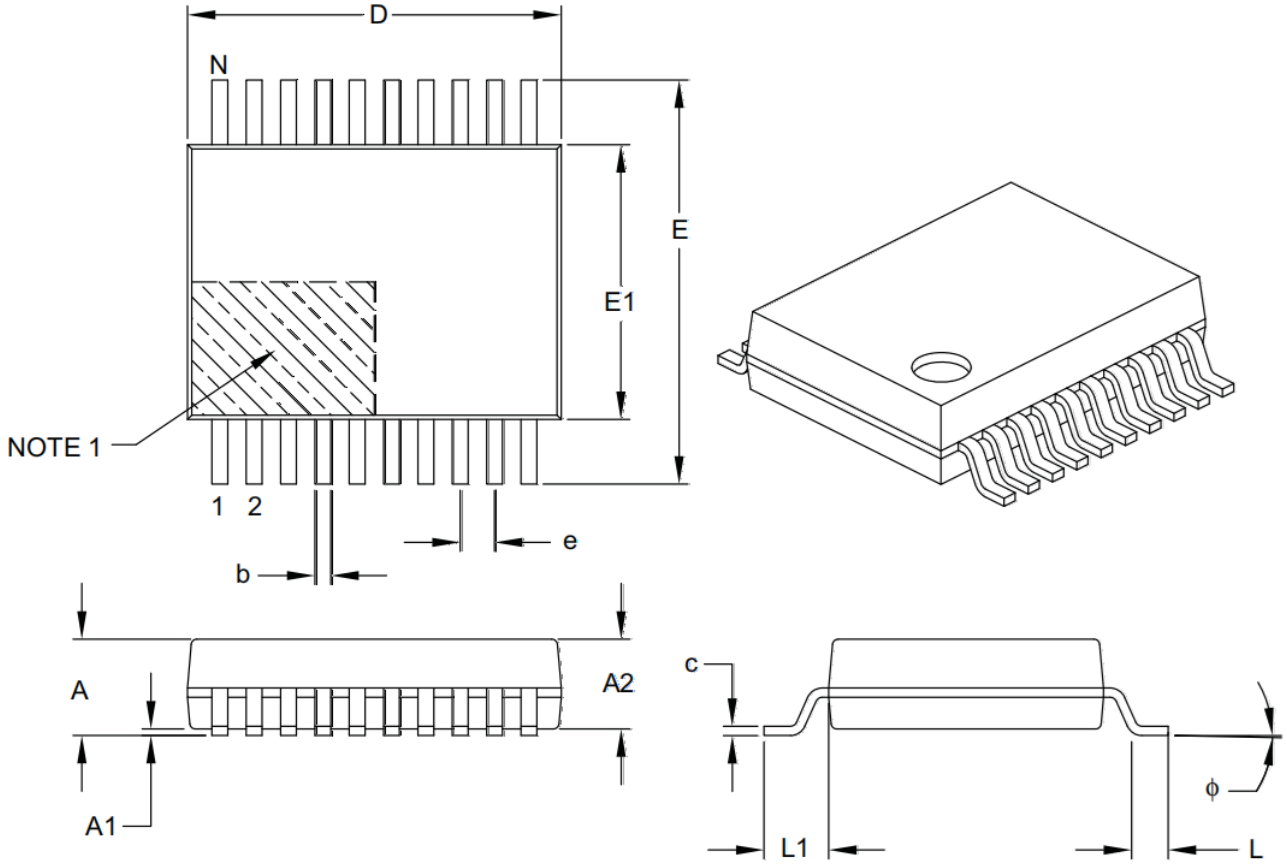
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width(X6)	X			0.60
Contact Pad Length(X6)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F666XI, 20-Lead Plastic Shrink Small Outline (SS) -5.30 mm[SSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.