Difmicro Technolog

DIF81F648

Datasheet

Content

DIF81F648 Features

High-Performance RISC CPU:

- Only **35** Instructions to Learn
  - All single-cycle instructions except branches
- Operating Speed:
  - **DC – 20 MHz** oscillator/clock input
  - **DC – 200 ns** instruction cycle
- Interrupt Capability
- **8**-level Deep Hardware Stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:

- Internal and External Oscillator Options
  - Precision Internal **4 MHz** oscillator factory calibrated to ±1%
  - External Oscillator support for crystals and resonators
  - **5** µs wake-up from Sleep, **3.0V**, typical
- Power-Saving Sleep mode
- Wide Operating Voltage Range **– 2.0V to 5.5V**
- Industrial and Extended Temperature Range
- Low-Power Power-on Reset (**POR**)
- Power-up Timer (**PWRT**) and Oscillator Start-up Timer (**OST**)
- Brown-out Detect (**BOD**)
- Watchdog Timer (**WDT**) with Independent Oscillator for Reliable Operation
- Multiplexed $\overline{\text{MCLR}}$/Input-pin
- Interrupt-on-Pin Change
- Individual Programmable Weak Pull-ups
- Programmable Code Protection
- High Endurance Flash/EEPROM Cell
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/data EEPROM retention: > 40 years

Low-Power Features:

- Standby Current:
  - **1nA @ 2.0V**, typical
- Operating Current:
  - **8.5µA @ 32 kHz, 2.0V**, typical
  - **100µA @ 1 MHz, 2.0V**, typical
- Watchdog Timer Current
  - **300nA @ 2.0V**, typical
- Timer1 Oscillator Current:
  - **4µ A @ 32 kHz, 2.0V**, typical

Peripheral Features:

- **12** I/O Pins with Individual Direction Control
  - High Current Sink/Source for Direct LED Drive
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip comparator voltage reference (CV_{REF}) module
  - Programmable input multiplexing from device inputs
  - Comparator output is externally accessible
- Analog-to-Digital Converter module:
  - **10-bit** resolution
  - Programmable 8-channel input
  - Voltage reference input
- Timer0: **8-bit** Timer/Counter with **8-bit**
- Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- In-Circuit Serial Programming (ICSP) via two pins

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)				
DIF81F648	1024	64	128	12	–	1	1/1

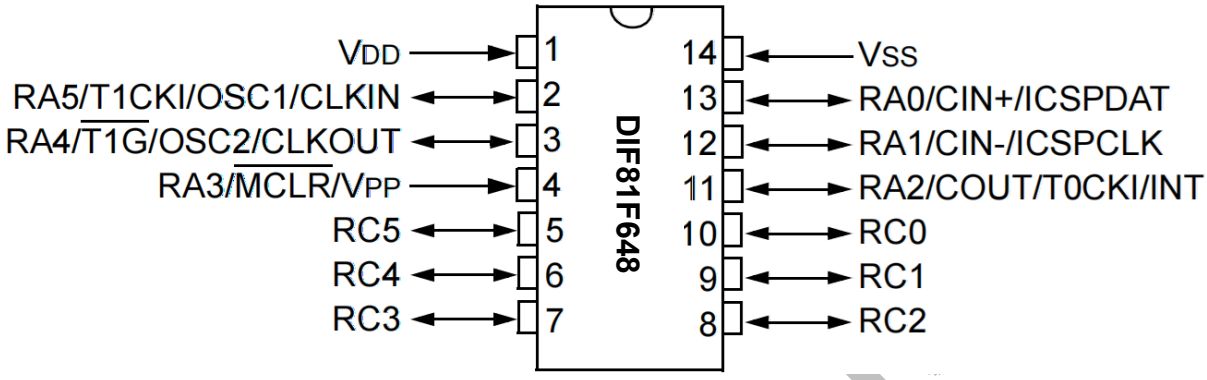
Pin Diagrams

DIF81F648 Pin Configurations:

DIF81F648DI(14-pin PDIP)

DIF81F648DI(14-pin SOIC)

DIF81F648DI(14-pin TSSOP)



CPU Kernel

DEVICE OVERVIEW

Figure *1* DIF81F648 BLOCK DIAGRAM。

Table 1 shows the pinout description.

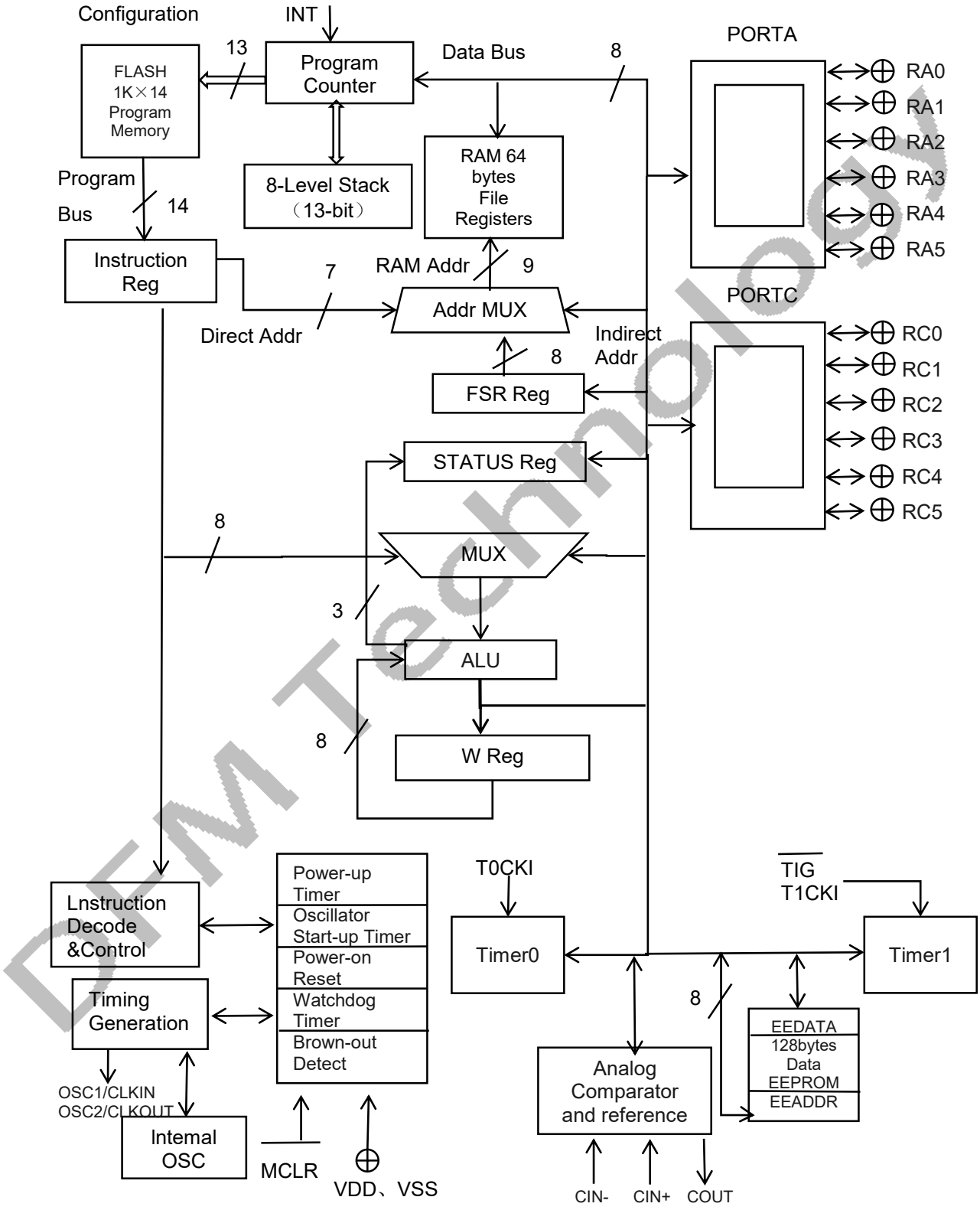


Figure 1.BLOCK DIAGRAM

Table 1.DIF81F648 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CIN+/ICSPDAT	RA0	TTL	CMOS	Bidirectional I/O w/ programmable pull-up and interrupt-on-change.
	—	—	—	A/D Channel 0 input.
	CIN+	AN		Comparator input.
	ICSPDAT	TTL	CMOS	Serial Programming Data I/O.
RA1/AN1/CIN-/VREF/ ICSPCLK	RA1	TTL	CMOS	Bidirectional I/O w/ programmable pull-up and
	—	—	—	A/D Channel 1 input.
	CIN-	AN	—	Comparator input.
	—	—	—	External Voltage reference.
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/AN2/COUT/T0CKI/INT	RA2	ST	CMOS	Bidirectional I/O w/ programmable pull-up and interrupt-on-change.
	—	—	—	A/D Channel 2 input.
	COUT	—	CMOS	Comparator output.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External Interrupt.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	Input port with interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear.
	VPP	HV	—	Programming voltage.
RA4/$\overline{\text{T1G}}$/AN3/OSC2/ CLKOUT	RA4	TTL	CMOS	Bidirectional I/O w/ programmable pull-up and interrupt-on-change.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	—	—	—	A/D Channel 3 input.
	OSC2	—	XTAL	Crystal/Resonator.
	CLKOUT	—	CMOS	Fosc/4 output.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	Bidirectional I/O w/ programmable pull-up and interrupt-on-change.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	Crystal/Resonator.
	CLKIN	ST	—	External clock input/RC oscillator connection.
RC0/AN4	RC0	TTL	CMOS	Bidirectional I/O.
	—	—	—	A/D Channel 4 input.
RC1/AN5	RC1	TTL	CMOS	Bidirectional I/O.
	—	—	—	A/D Channel 5 input.
RC2/AN6	RC2	TTL	CMOS	Bidirectional I/O.
	—	—	—	A/D Channel 6 input.
RC3/AN7	RC3	TTL	CMOS	Bidirectional I/O.
	—	—	—	A/D Channel 7 input.
RC4	RC4	TTL	CMOS	Bidirectional I/O.
RC5	RC5	TTL	CMOS	Bidirectional I/O.
VSS	VSS	电源	—	Ground reference.
VDD	VDD	电源	—	Positive supply.

Legend:

TTL = TTL input buffer

ST = Schmitt Trigger input buffer

MEMORY ORGANIZATION

Program Memory Organization

The DIF81F648 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the DIF81F648 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

Data Memory Organization

The data memory is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

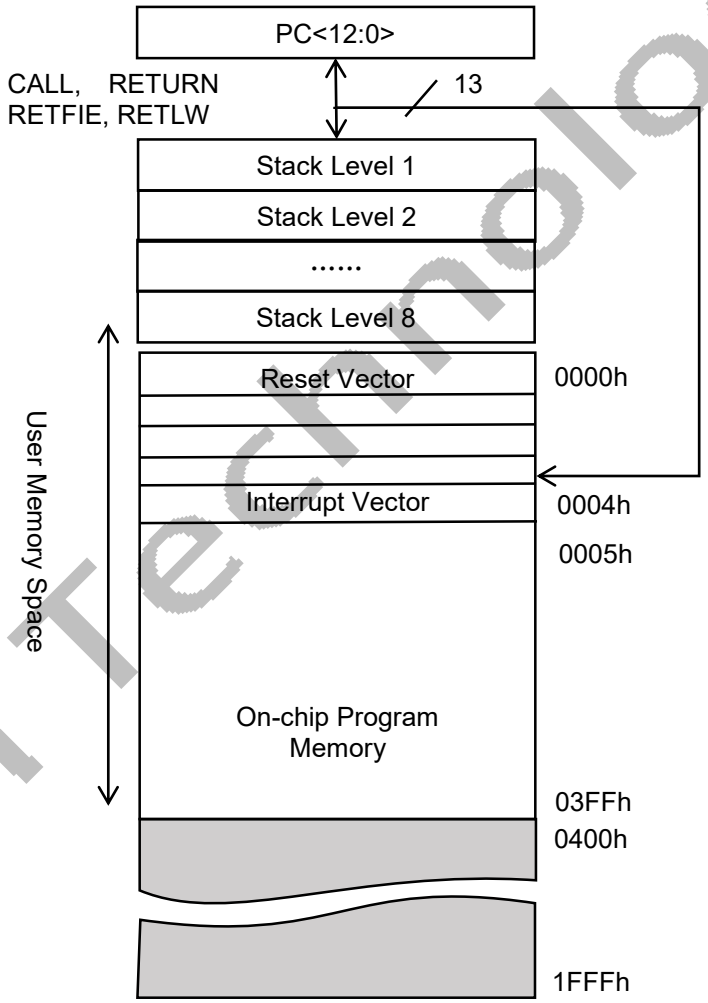


Figure 2.PROGRAM MEMORY MAP AND STACK FOR THE DIF81F648

GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 in the DIF81F648 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR

SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

Indirect Addr	00h	Indirect Addr	80h
PCL	01h	OPTION REG	81h
STATUS	02h	PCL	82h
FSR	03h	FSR	83h
PORTA	04h	TRISA	84h
	05h		85h
PORTC	06h	TRISC	86h
	07h		87h
	08h		88h
PCLATH	09h	PCLATH	89h
INTCON	0Ah	INTCON	8Ah
PIR1	0Bh	PIE1	8Bh
	0Ch		8Ch
TMR1L	0Dh	PCON	8Dh
TMR1H	0Eh		8Eh
T1CON	0Fh	OSCCAL	8Fh
	10h	ANSEL	90h
	11h		91h
	12h		92h
	13h		93h
	14h		94h
	15h		95h
	16h		96h
	17h		97h
	18h		98h
	19h		99h
CMCON	1Ah	VRCON	9Ah
	1Bh	EEDAT	9Bh
	1Ch	EEADR	9Ch
	1Dh	EECON1	9Dh
	1Eh	EECON2	9Eh
	1Fh		9Fh
ADRESH	20h	ADRESL	A0h
ADCON0	5Fh	ADCON1	DFh
GENERAL PURPOSE REGISTER 64 字节		Accesses 20h-5Fh	
Bank 0		Bank 1	

Figure 3.DATA MEMORY MAP OF THE DIF81F648

Table 2.DIF81F648 SPECIAL REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	IRP(2)	RP1(2)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
04h	FSR	Indirect data memory Address Pointer								xxxx xxxx
05h	PORTA	—	—	I/O Control Registers						--xx xxxx
06h	—	Unimplemented								–
07h	PORTC	—	—	I/O Control Registers						--xx xxxx
08h	—	Unimplemented								–
09h	—	Unimplemented								–
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0
0Dh	—	Unimplemented								–
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx
10h	T1CON	—	T1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	-000 0000
11h	—	Unimplemented								–
12h	—	Unimplemented								–
13h	—	Unimplemented								–
14h	—	Unimplemented								–
15h	—	Unimplemented								–
16h	—	Unimplemented								–
17h	—	Unimplemented								–
18h	—	Unimplemented								–
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000
1Ah	—	Unimplemented								–
1Bh	—	Unimplemented								–
1Ch	—	Unimplemented								–
1Dh	—	Unimplemented								–
1Eh	—	Unimplemented								xxxx xxxx
1Fh	—	Unimplemented								00-0 0000

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

Note 1: Other (NON Power-up) Resets include MCLR Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

2: IRP and RP1 bits are reserved, always maintain these bits clear.

TABLE 2-2: DIF81F648 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD
Bank 1										
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	IRP(2)	RP1(2)	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx
84h	FSR	Indirect data memory Address Pointer								xxxx xxxx
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111
86h	—	Unimplemented								–
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111
88h	—	Unimplemented								–
89h	—	Unimplemented								–
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0
8Dh	—	Unimplemented								–
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$	---- --qq
8Fh	—									–
90h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--
91h	—	Unimplemented								1111 1111
92h		Unimplemented								–
93h	—	Unimplemented								–
94h	—	Unimplemented								–
95h	WPUA	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000
97h	—	Unimplemented								–
98h	—	Unimplemented								–
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000
9Ah	EEDAT	EEPROM data register								0000 0000
9Bh	EEADR	—	EEPROM address register							0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000
9Dh	EECON2	EEPROM control register 2 (not a physical register)								---- ----
9Eh	—	Unimplemented								xxxx xxxx
9Fh	—	Unimplemented								-000 ----

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

2: IRP and RP1 bits are reserved, always maintain these bits clear.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias.....-40 to +125°C
Storage temperature..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}.....-0.3Vto +6.5V
Voltage on MCLR with respect to Vss.....-0.3V.to +13.5V
Voltage on all other pins with respect to V_{SS}.....0.3V to (V_{DD} + 0.3V)
Total power dissipation(1).....800 mW
Maximum current out of V_{SS} pin.....300 mA
Maximum current into V_{DD} pin.....250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}).....± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}).....± 20 mA
Maximum output current sunk by any I/O pin.....25 mA
Maximum output current sourced by any I/O pin.....25 mA
Maximum current sunk by PORTA and PORTC (combined).....200 mA
Maximum current sourced PORTA and PORTC (combined).....200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OI} \times I_{OL})$.

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

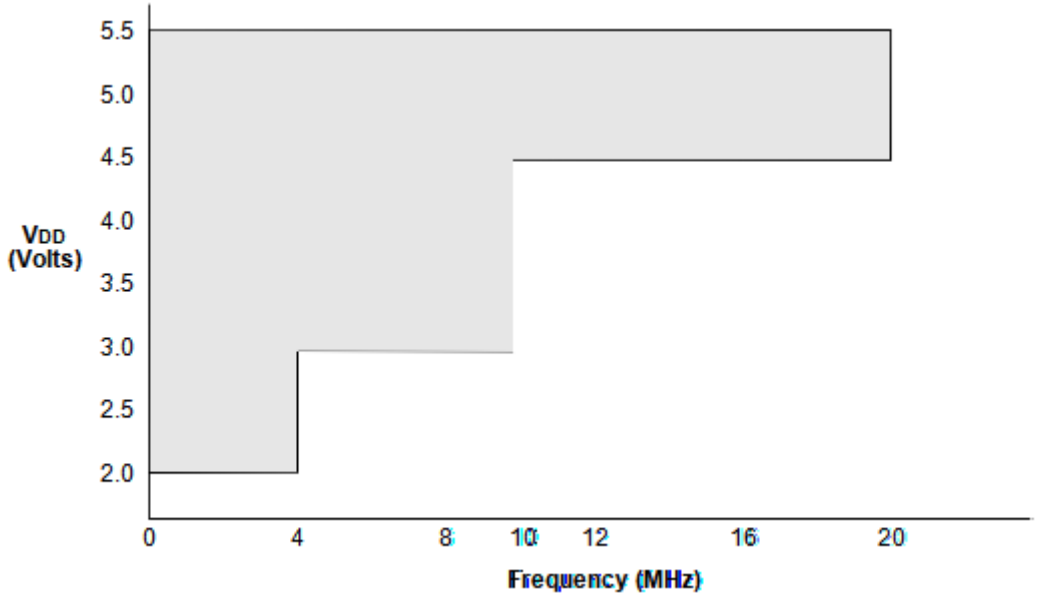


Figure **4.**DIF81F648 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH,-40℃ ≤ TA ≤ +125℃

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

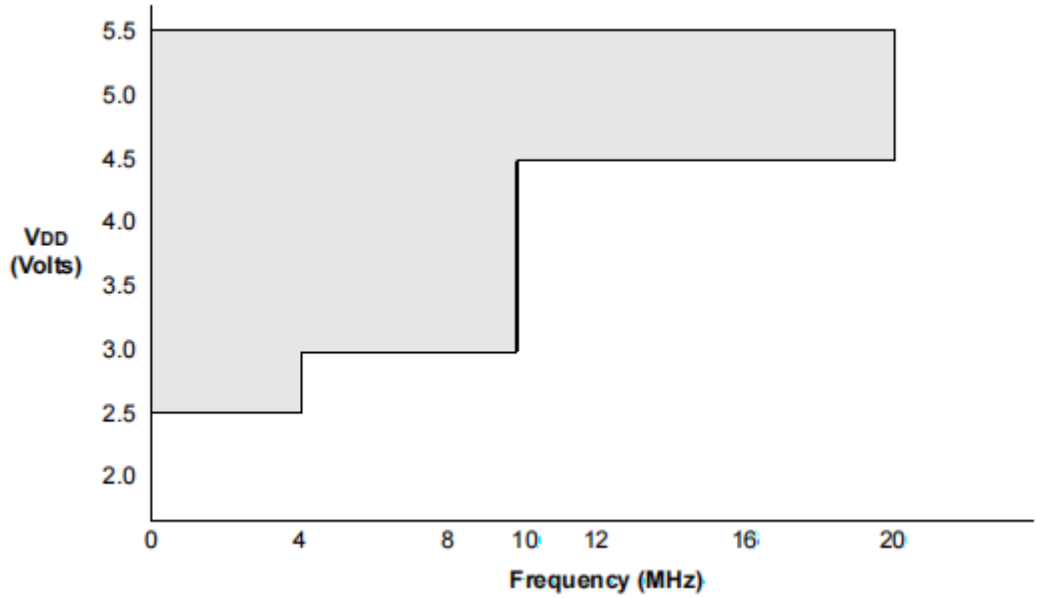


Figure **5.**DIF81F648 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,-40℃ ≤ TA ≤ +125℃

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

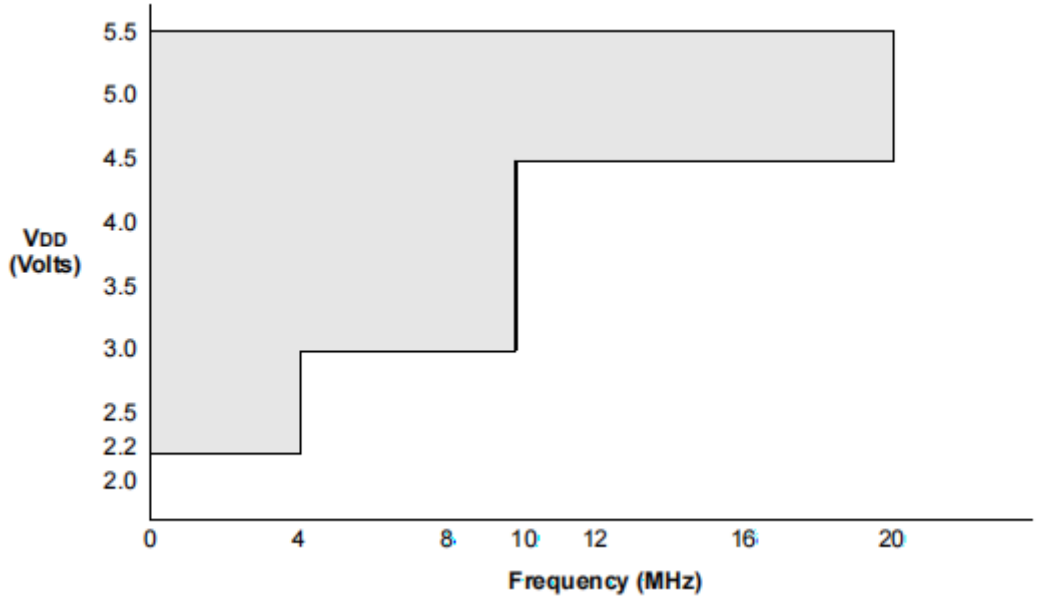


Figure **6.**DIF81F648 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,-40° C ≤ TA ≤ +125° C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

DC Characteristics: DIF81F648

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	FOSC < = 4 MHz: DIF81F648 with A/D off
D001A			2.2		5.5	V	DIF81F648 with A/D on, 0°C to +125°C
D001B			2.5		5.5	V	DIF81F648 with A/D on, -40°C to +125°C
D001C			3.0		5.5	V	4 MHz < FOSC < = 10 MHz
D001D			4.5		5.5	V	
D002	VDR	**RAM Data Retention Voltage**(1)	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	
D005	VBOD		—	2.1	—	V	

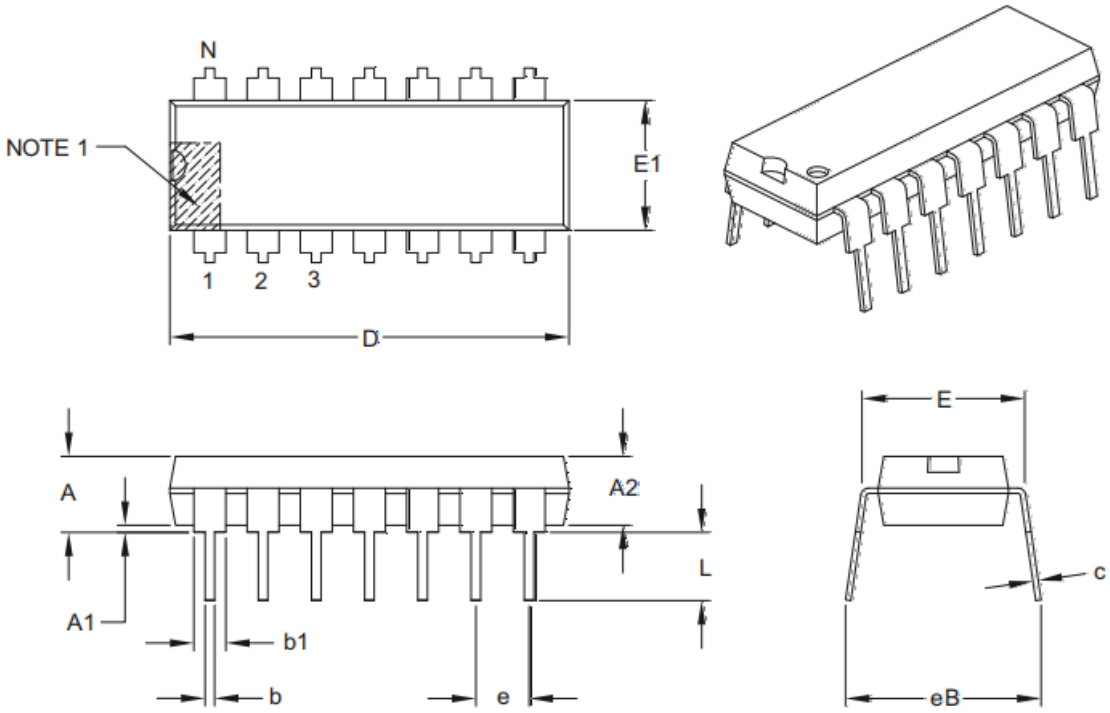
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

Package Details

DIF81F648DI, 14-Lead Plastic Dual In-Line (P) – 300 mil Body [DIP]



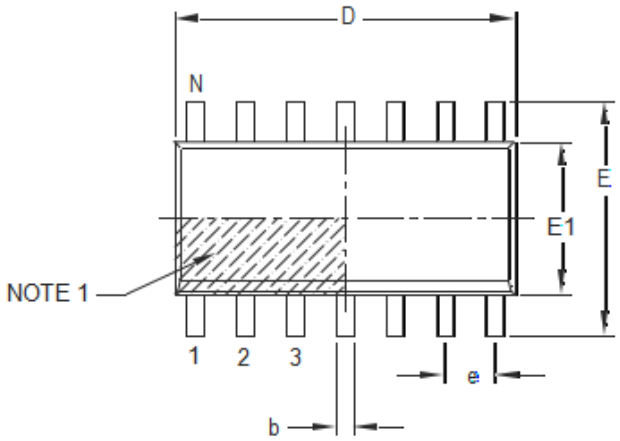
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

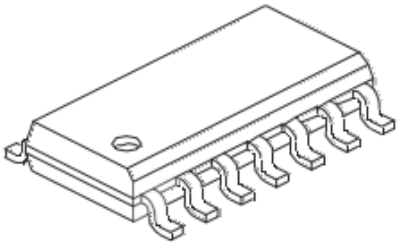
Notes:

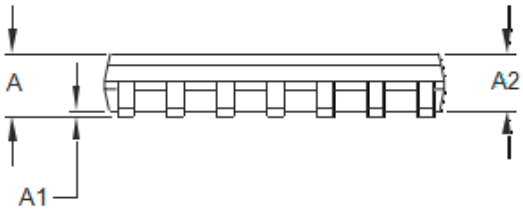
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

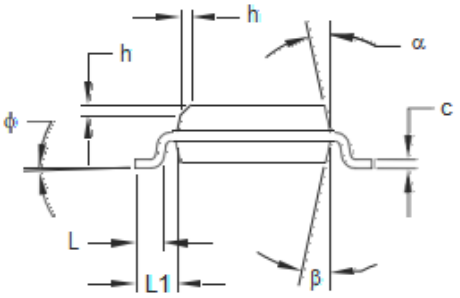
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F648SI, 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

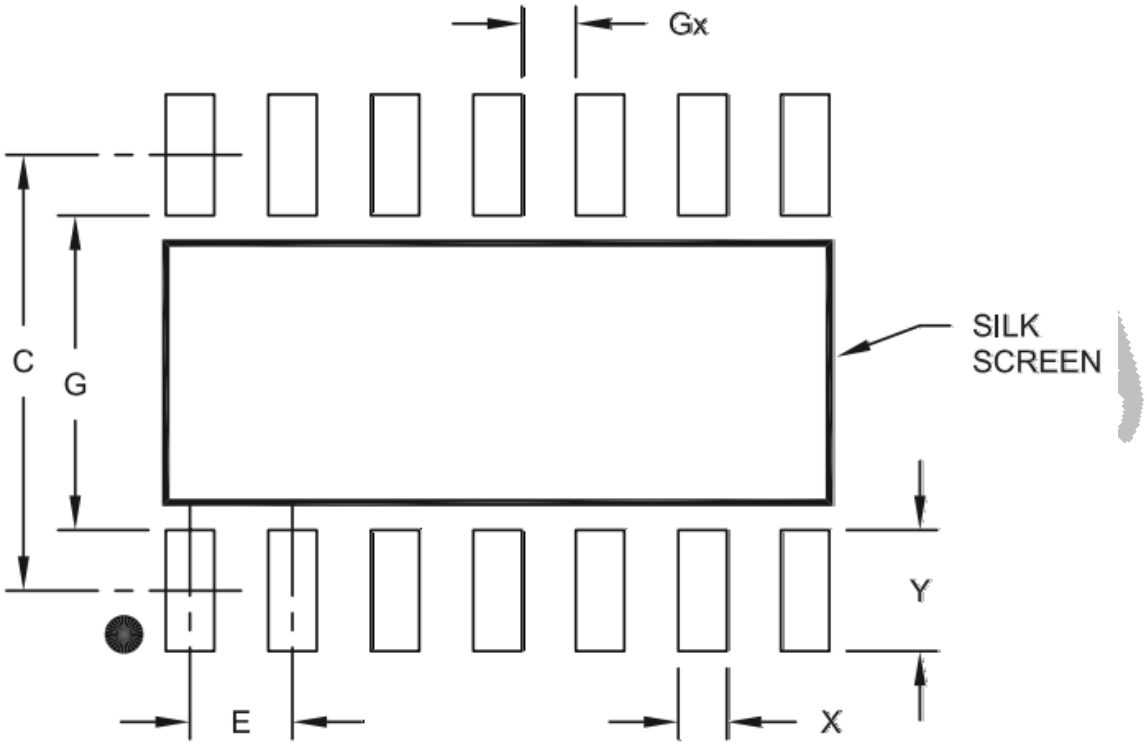
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F648SI, 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

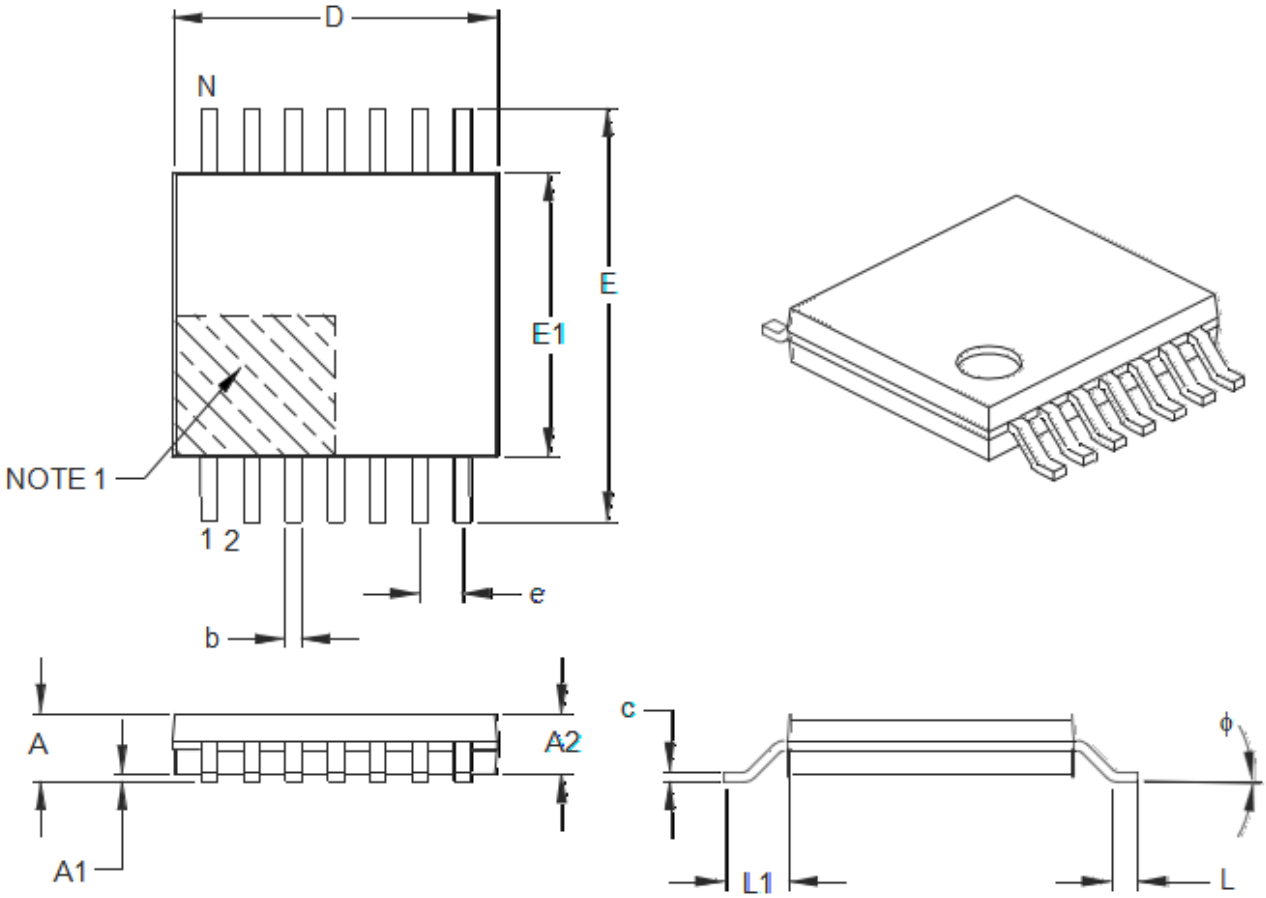
Units		MILLIMETERS		
Dimension Limits		Min	MON	MAX
Contact Pitch	E		1.27BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F648TI, 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]



Units		MILLIMETERS		
Dimension Limits		Min	MON	MAX
Number of Pins	N		14	
Pitch	e		0.65BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

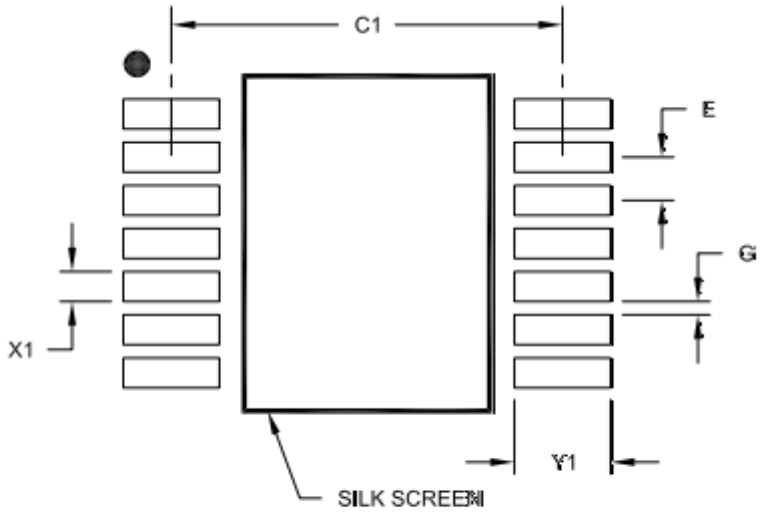
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F648TI, 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		Min	MON	MAX
Contact Pitch	E	0.65BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width(X14)	X1			0.45
Contact Pad Length(X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.