Difmicro Technolog

DIF81F1843

Datasheet

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DIF81F1843 Product characteristics

High-Performance RISC CPU:

- Only 49 Instructions to learn
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4xPLL
  - 3 external clock modes up to 32 MHz
- 4x Phase Locked Loop (PLL)
- Fail-Safe Clock Monitor
- Two-Speed Start-up
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-Up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming (ICSP) via two pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 5.5V
- Programmable Code Protection
- Self-Programmable under Software Control

Low-Power Features/CMOS Technology:

- Standby Current:
  - 30 nA @ 1.8V, typical
- Operating Current:
  - 75 A @ 1 MHz, 1.8V, typical
- Low-Power Watchdog Timer Current :
  - 500 nA @ 1.8V, typical

Peripheral Features:

- Up to 17 I/O Pins and 1 Input-only Pin:
  - High current sink/source for LED drivers
  - Individually programmable interrupt-on- change pins
  - Individually programmable weak pull-ups
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Up to three Timer2 modules (Timer2,4,6): 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Up to two Enhanced Capture, Compare, PWM modules (ECCP):
  - Software selectable time-bases
  - Auto-shutdown and auto-restart
  - PWM steering
- Up to two Capture, Compare, PWM modules (CCP):
  - Software selectable time-bases
- Up to two Master Synchronous Serial Port (MSSP) with SPI and I2C with:
  - 7-bit address masking
  - SMBus/PMBus compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start
- SR Latch (Integrated 555 Timer):
  - Multiple Set/Reset input options
- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 12 channels
- Up to 2 Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference module:
  - Fixed voltage reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection
- Capacitive Touch oscillator module:
  - Up to 12 channels
- Data Signal Modulator:
  - Select modulator and carrier sources from various module outputs.

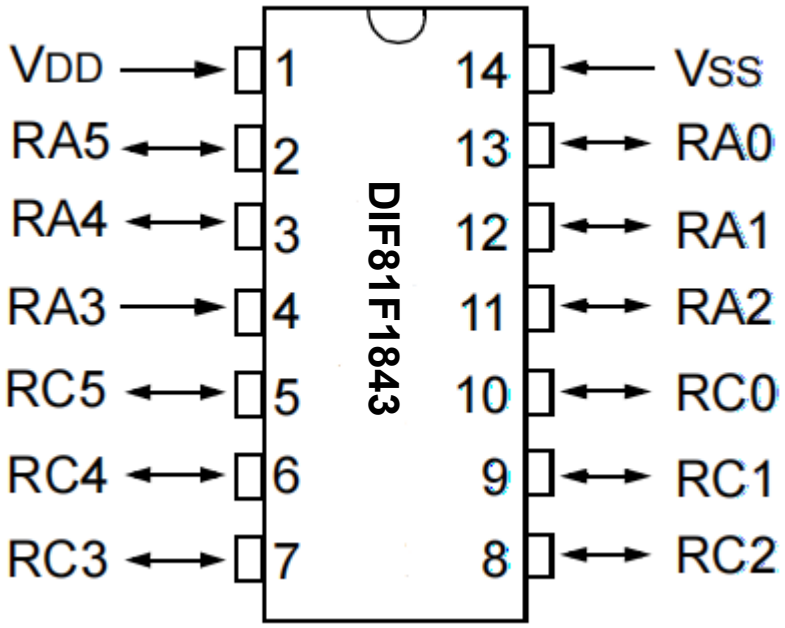
Table 1.DIF81F1843

Device	Program Memory Flash (words)	Data EEPROM (bytes)	SRAM (bytes)	I/Os	10-bit A/D (ch)	Timers 8/16-bit	EUSART	MSSP	ECCP/ CCP	Cap Touch Channels
DIF81F1843	8192	256	1024	12	8	4/1	1	1	2/2	8

Pin Diagrams

DIF81F1843SI(14-pin SOP)

DIF81F1843TI(14-pin TSOP)



DIF81F1843NI(16-pin QFN)

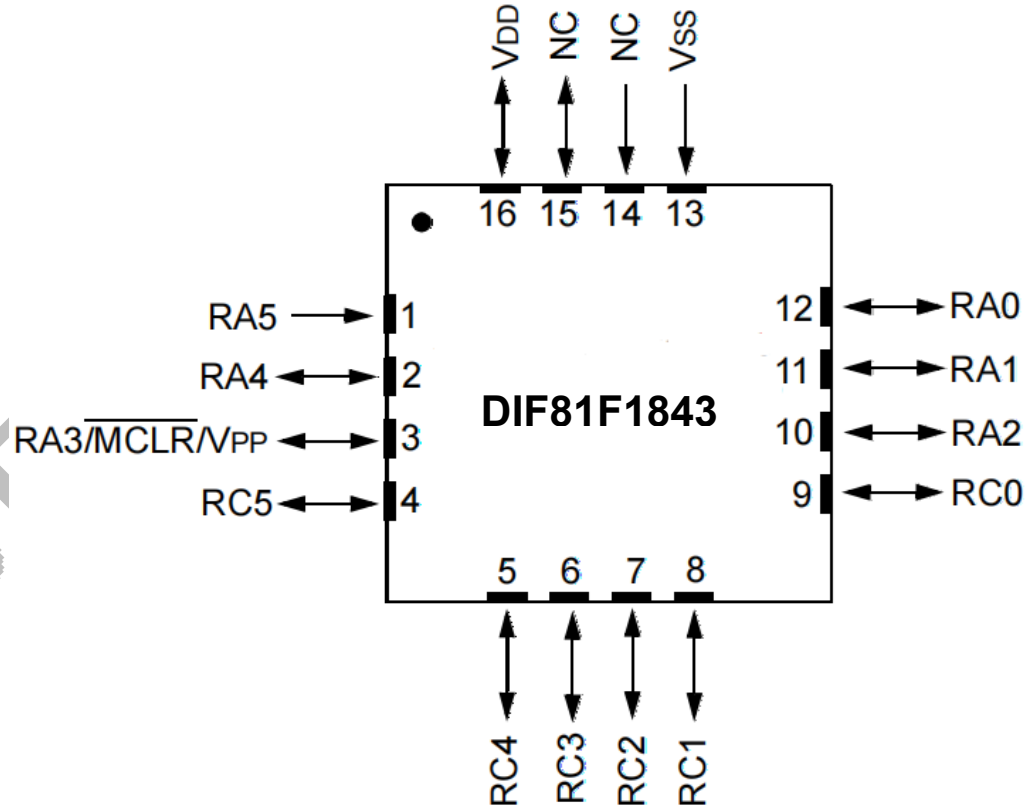


Table 2. 14-PIN AND 16-PIN ALLOCATION TABLE (DIF81F1843)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	MSSP	Interrupt	Modulator	Pull-up	Basic
RA0	13	7	AN0	DACOUT	CPS0	C1IN+	—	—	—	TX(1) CK(1)	—	IOC	—	Y	ICSPDAT/ ICDDAT
RA1	12	11	AN1	VREF	CPS1	C12IN0-	SRI	—	—	RX(1) DT(1)	—	IOC	—	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	—	CPS2	C1OUT	SRQ	T0CKI	CCP3(2) FLT0	—	—	INT/ IOC	—	Y	—
RA3	4	3	—	—	—	—	—	T1G(1)	—	—	$\overline{SS}$(1)	IOC	—	Y	$\overline{MCLR}$ VPP
RA4	3	2	AN3	—	CPS3	—	—	T1G(1) T1OSO	P2B(1,2)	—	SDO(1)	IOC	—	Y	OSC2 CLKOUT CLKR
RA5	2	1	—	—	—	—	—	T1CKI T1OSI	CCP2(1,2) P2A(1,2)	—	—	IOC	—	Y	OSC1 CLKIN
RC0	10	9	AN4	—	CPS4	C2IN+	—	—	P1D(1,2)	—	SCL SCK	—	—	Y	—
RC1	9	8	AN5	—	CPS5	C12IN1-	—	—	P1C(1,2) CCP4(2)	—	SDA SDI	—	—	Y	—
RC2	8	7	AN6	—	CPS6	C12IN2-	—	—	P1D(1) P2B(1,2)	—	SDO(1)	—	MDCIN1	Y	—
RC3	7	6	AN7	—	CPS7	C12IN3-	—	—	P1C(1) CCP2(1,2) P2A(1,2)	—	$\overline{SS}$(1)	—	MDMIN	Y	—
RC4	6	5	—	—	—	C2OUT	SRNQ	—	P1B	TX(1) CK(1)	—	—	MDOUT	Y	—
RC5	5	4	—	—	—	—	—	—	CCP1 P1A	RX(1) DT(1)	—	—	MDCIN2	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin functions can be assigned to one of two pin locations via software.

2: Pin function only available on DIF81F1843.

CPU Kernel

DEVICE OVERVIEW

The DIF81F1843 are described within this data sheet. They are available in 14/16 pin packages. **Figure 1** shows a block diagram of the DIF81F1843 devices. Reference ***Table 3*** for peripherals available per device.

Table 3.DEVICE PERIPHERAL SUMMARY

Peripheral		DIF81F1843
ADC		•
Capacitive Sensing (CPS) Module		•
Data EEPROM		•
Digital-to-Analog Converter (DAC)		•
Digital Signal Modulator (DSM)		•
EUSART		•
Fixed Voltage Reference (FVR)		•
SR Latch		•
	ECCP1	•
	ECCP2	•
	CCP3	•
	CCP4	•
	C1	•
	C2	•
	MSSP1	•
	MSSP2	
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•
	Timer6	•

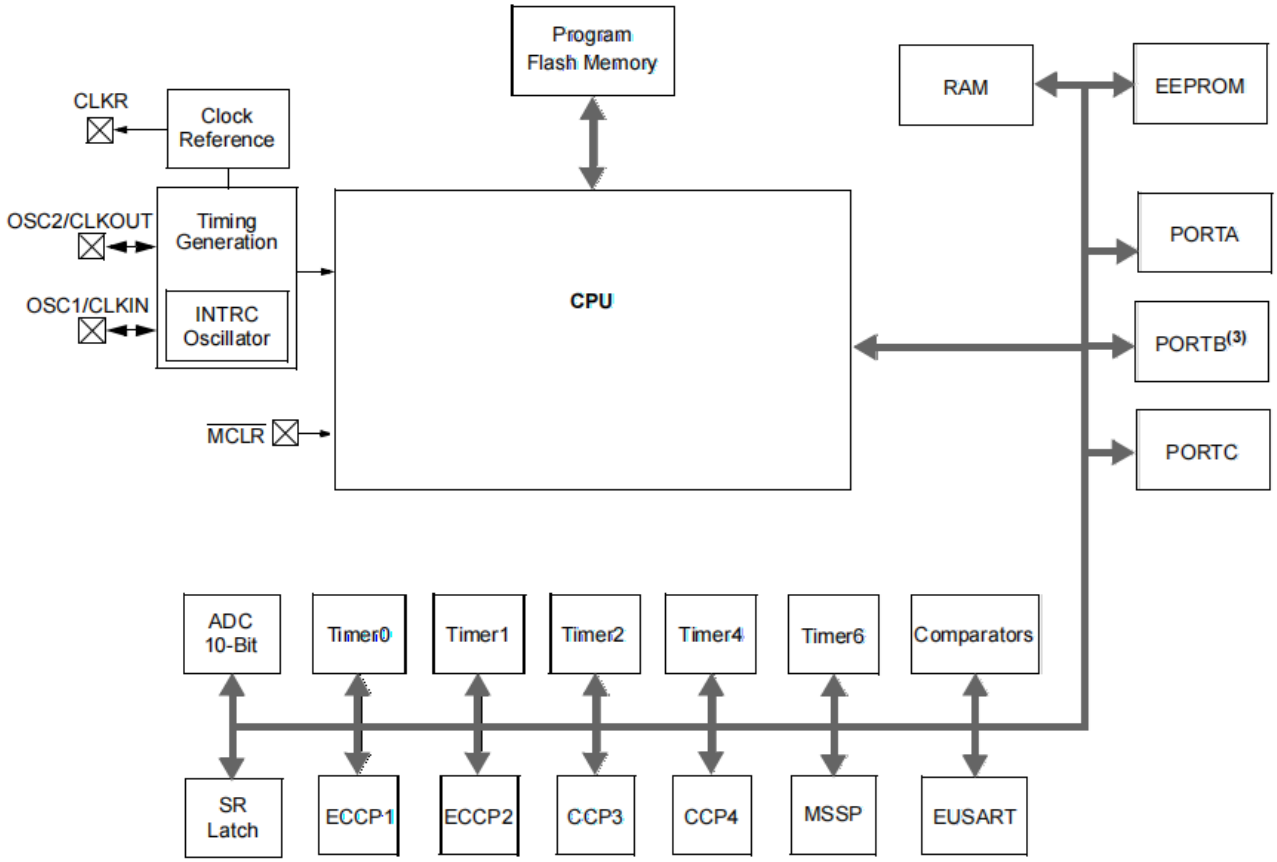


Figure 1. DIF81F1843 BLOCK DIAGRAM

Note **1: See applicable chapters for more information on peripherals.**

2: See *Table 3* for peripherals available on specific devices.

Table 4. DIF81F1843 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/ DACOUT/TX(1)/CK(1)/ ICSPDAT/ICDDAT	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	CPS0	AN	—	Capacitive sensing input 0.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	—	AN	Digital-to-Analog Converter output.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	ICSPDAT	ST	CMOS	ICSP Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/ SRI/RX(1)/DT(1)/ICSPCLK/ ICDCLK	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPS1	AN	—	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	—	SR Latch input.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/ C1OUT/SRQ/CCP3/FLT0	RA2	ST	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
	SRQ	—	CMOS	SR Latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM 3.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RA3/SS1(1)/T1G(1)/VPP/ MCLR	RA3	TTL	—	General purpose input.
	SS1	ST	—	Slave Select input.
	T1G	ST	—	Timer1 Gate input.
	VPP	HV	—	Programming voltage.
	MCLR	ST	—	Master Clear with internal pull-up.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST= Schmitt Trigger input with CMOS levels I2C = Schmitt Trigger input with I2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

2: Default function location.

Table 5. DIF81F1843 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA4/AN3/CPS3/OSC2/CLKOUT/T1OSO/CLKR/SDO(1)/ P2B(1)/T1G(1,2)	RA4	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	CPS3	AN	—	Capacitive sensing input 3.
	OSC2	—	CMOS	Comparator C2 output.
	CLKOUT	—	CMOS	Fosc/4 output.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	CLKR	—	CMOS	Clock Reference output.
	SDO	—	CMOS	SPI data output.
	P2B	—	CMOS	PWM output.
	T1G	ST	—	Timer1 Gate input.
RA5/CLKIN/OSC1/T1OSI/T1CKI/P2A(1)/CCP2(1)	RA5	TTL	CMOS	General purpose I/O.
	CLKIN	CMOS	—	External clock input (EC mode).
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RC0/AN4/CPS4/C2IN+/SCL/ SCK/P1D(1)	RC0	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS4	AN	—	Capacitive sensing input 4.
	C2IN+	AN	—	Comparator C2 positive input.
	SCL	I^2C	OD	I^2C™ clock.
	SCK	ST	CMOS	SPI clock.
	P1D	—	CMOS	PWM output.
RC1/AN5/CPS5/C12IN1-/SDA/SDI/P1C(1)/CCP4	RC1	TTL	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	—	Capacitive sensing input 5.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
	SDA	I^2C	OD	I^2C data input/output.
	SDI	CMOS	—	SPI data input.
	P1C	—	CMOS	PWM output.
	CCP4	AN	—	Capacitive sensing input 4.
RC2/AN6/CPS6/C12IN2-/P1D(1,2)/P2B(1,2)/SDO(1,2)/ MDCIN1	RC2	TTL	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	CPS6	AN	—	Capacitive sensing input 6.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	SDO	—	CMOS	SPI data output.
	MDCIN1	ST	—	Modulator Carrier Input 1.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST= Schmitt Trigger input with CMOS levels I2C = Schmitt Trigger input with I2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

2: Default function location.

Name	Function	Input Type	Output Type	Description
RC3/AN7/CPS7/C12IN3-/P2A(1,2)/CCP2(1,2)/ P1C(1,2)/ $\overline{SS1}$(1,2)/MDMIN	RC3	TTL	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	CPS7	AN	—	Capacitive sensing input 7.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	P2A	—	CMOS	PWM output.
	CCP2	AN	—	Capacitive sensing input 2.
	P1C	—	CMOS	PWM output.
	$\overline{SS1}$	ST	—	Slave Select input.
	MDMIN	ST	—	Modulator source input.
RC4/C2OUT/SRNQ/P1B/TX(1,2)/CK(1,2)/MDOUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	SRNQ	—	CMOS	SR Latch inverting output.
	P1B	—	CMOS	PWM output.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	MDOUT	—	CMOS	Modulator output.
RC5/P1A/CCP1/DT(1,2)/RX(1,2)/MDCIN2	RC5	TTL	CMOS	General purpose I/O.
	P1A	—	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM 1.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	MDCIN2	ST	—	Modulator Carrier Input 2.
VDD	V_{DD}	Power	—	Positive supply.
VSS	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST= Schmitt Trigger input with CMOS levels I2C = Schmitt Trigger input with I2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.

2: Default function location.

ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, indirect, and relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code.

16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Under- flow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a soft- ware Reset.

File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs.

Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU.

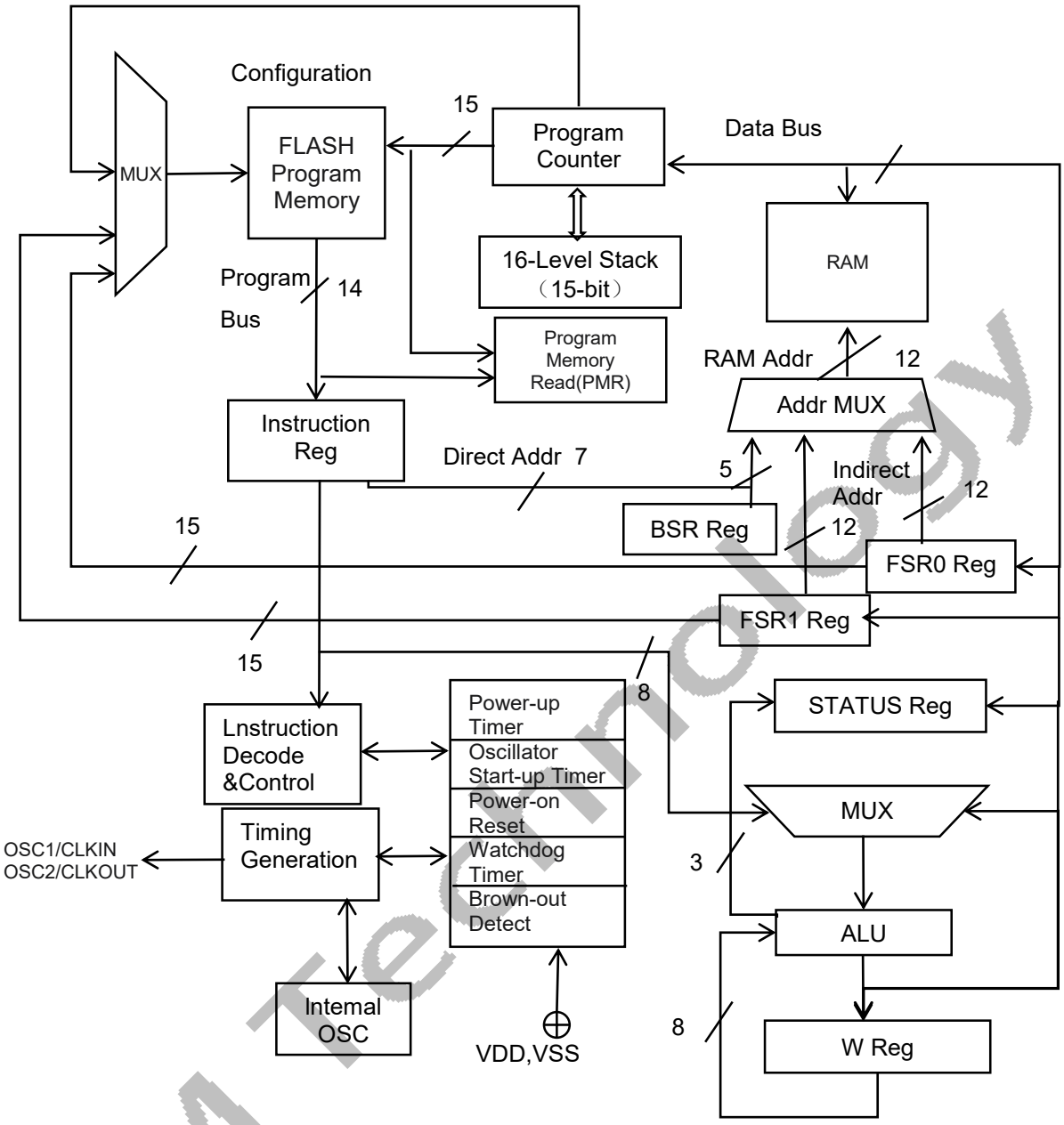


Figure 2. DIF81F1843 CORE BLOCK DIAGRAM

MEMORY ORGANIZATION

There are three types of memory in DIF81F1843 devices: Data Memory, Program Memory and Data EEPROM Memory.

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. ***Table 6*** shows the memory sizes implemented for the DIF81F1843 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers.

Table 6.DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
DIF81F1843	8,192	7FFFh

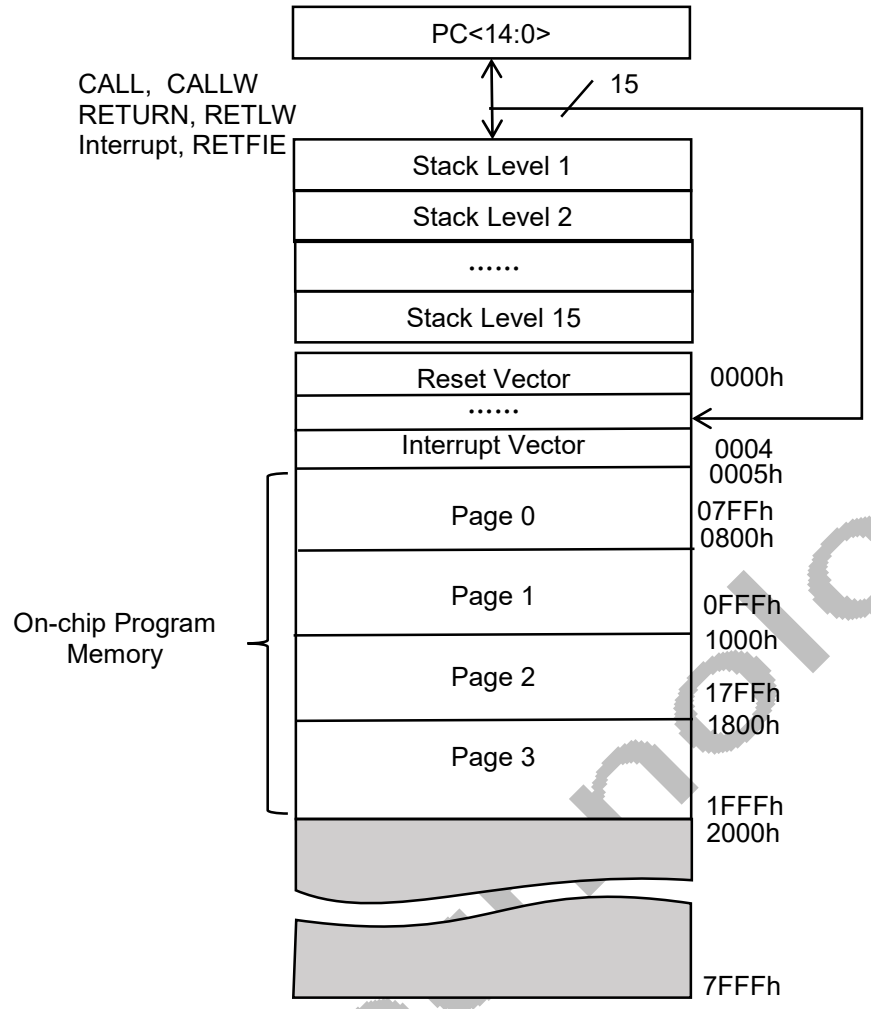


Figure 3. PROGRAM MEMORY MAP AND STACK FOR DIF81F1843

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias..... -40°C to +125°C
Storage temperature..... -65°C to +150°C
Voltage on VDD with respect to VSS, DIF81F1843.....-0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss.....-0.3V to +9.0V
Voltage on all other pins with respect to VSS.....0.3V to (VDD + 0.3V)
Total power dissipation(1).....800 mW
Maximum current out of VSS pin, -40°C≤TA≤+85°C for industrial.....85 mA
Maximum current out of VSS pin, -40°C≤TA≤+125°C for extended.....35 mA
Maximum current into VDD pin, -40°C≤TA≤ +85°C for industrial.....800 mA
Maximum current into VDD pin, -40°C≤TA≤+125°C for extended.....30 mA
Clamp current, IK (VPIN < 0 or VPIN > VDD.....20 mA
Maximum output current sunk by any I/O pin.....25 mA
Maximum output current sourced by any I/O pin.....25 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

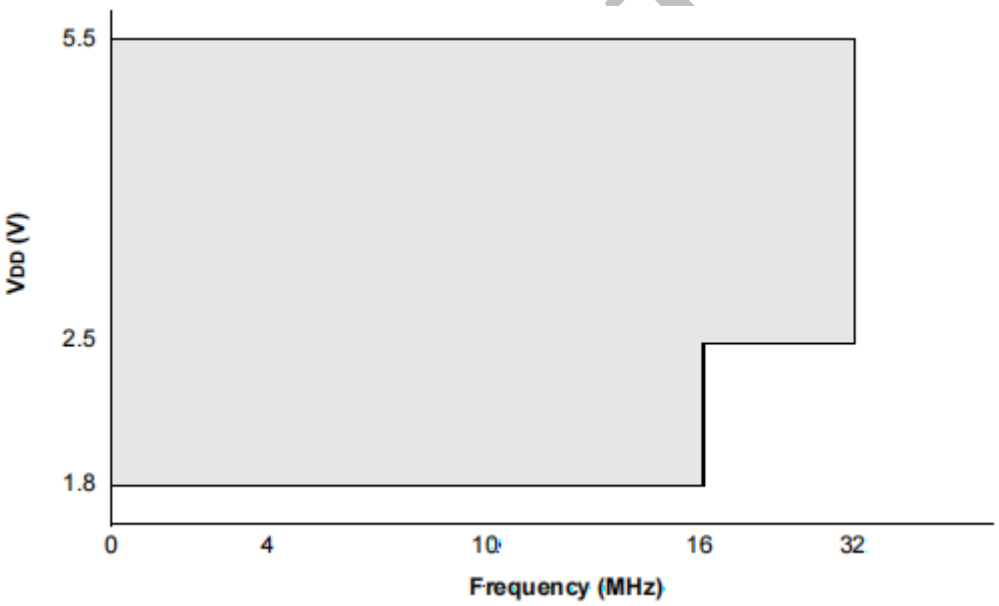


Figure 4. DIF81F1843 VOLTAGE FREQUENCY GRAPH, -40°C≤TA≤+125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

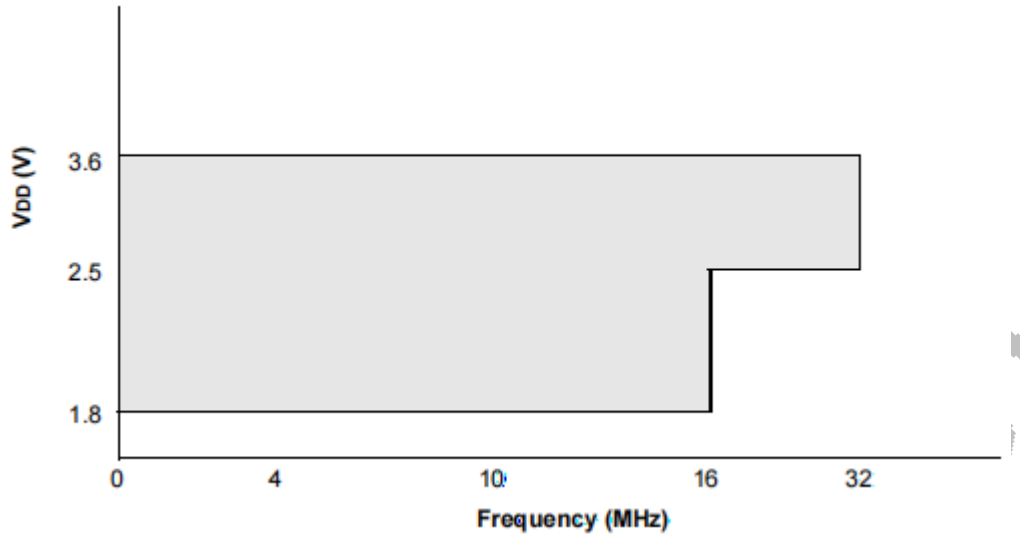


Figure 5. DIF81F1843 VOLTAGE FREQUENCY GRAPH, -40°C≤TA≤+125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency

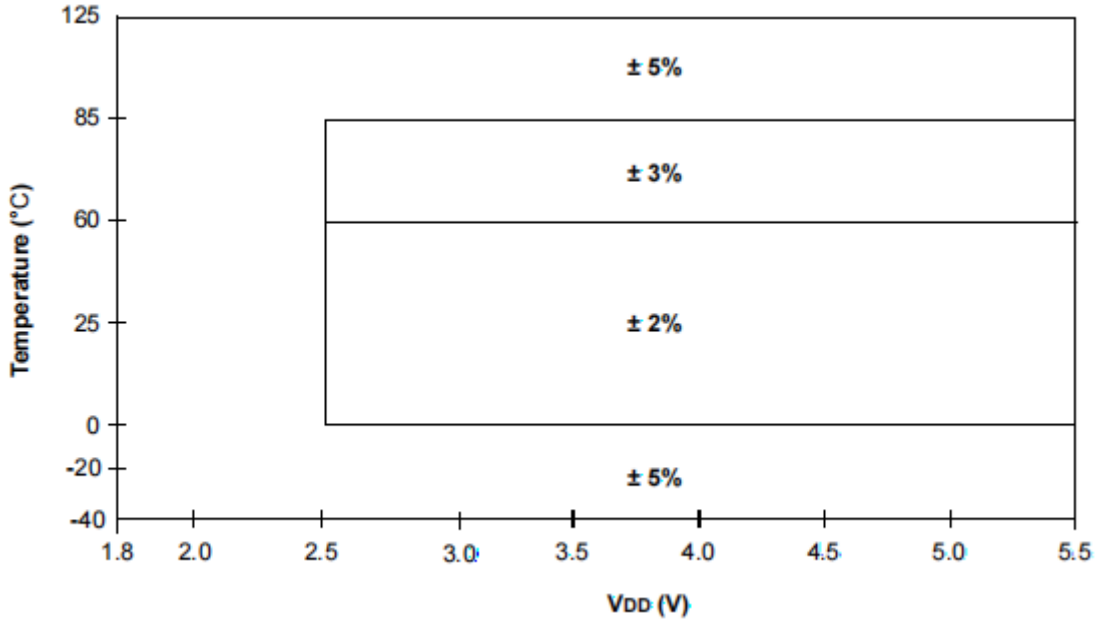


Figure 6. HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

DC Characteristics: DIF81F1843-I/E

DIF81F1843			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage(VDDMIN, VDDMAX)**					
D001		DIF81F1843	1.8 2.3	— —	5.5 5.5	V V	FOSC ≤ 16 MHz: FOSC ≤ 32 MHz (**NOTE 2**)
D002*	VDR	**RAM Data Retention Voltage(1)**					
D002*		DIF81F1843	1.7	—	—	V	Device in Sleep mode
	VPOR*	**Power-on Reset Release Voltage**	—	1.6	—	V	
D002B*	VPORR*	**Power-on Reset Rearm Voltage**					
		DIF81F1843	—	1.7	—	V	Device in Sleep mode
D003	VADFVR	**Fixed Voltage Reference Voltage for ADC, Initial Accuracy**	-8	—	6	%	1.024V, VDD ≥ 2.5V 2.048V, VDD ≥ 2.5V 4.096V, VDD ≥ 4.75V
D003A	VCDAFVR	**Fixed Voltage Reference Voltage for Comparator and DAC, Initial Accuracy**	-11	—	7	%	1.024V, VDD ≥ 2.5V 2.048V, VDD ≥ 2.5V 4.096V, VDD ≥ 4.75V
D003C*	TCVFVR	**Temperature Coefficient, Fixed Voltage Reference**	—	-130	—	ppm/°C	
D003D*	ΔVFVR/ ΔVIN	**Line Regulation, Fixed Voltage Reference**	—	0.270	—	%/V	
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	

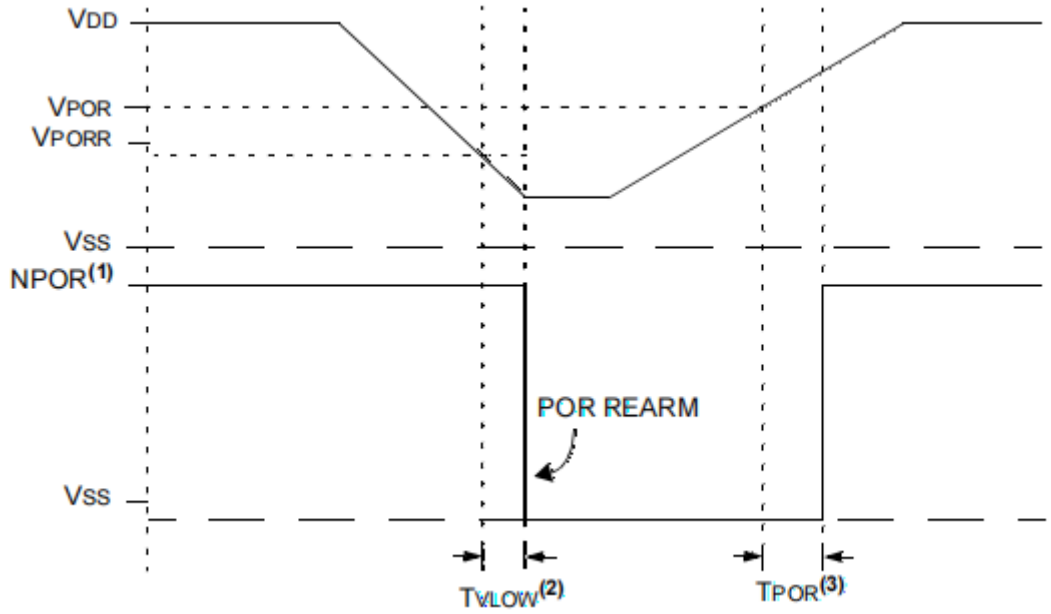
* These parameters are characterized but not tested.

Data in “Typ” column is at 3.0V, 25° C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note **1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

3: For proper operation, the minimum value of the ADC positive voltage reference must be 1.8V or greater. When selecting the FVR or the VREF+ pin as the source of the ADC positive voltage reference, be aware that the voltage must be 1.8V or greater.



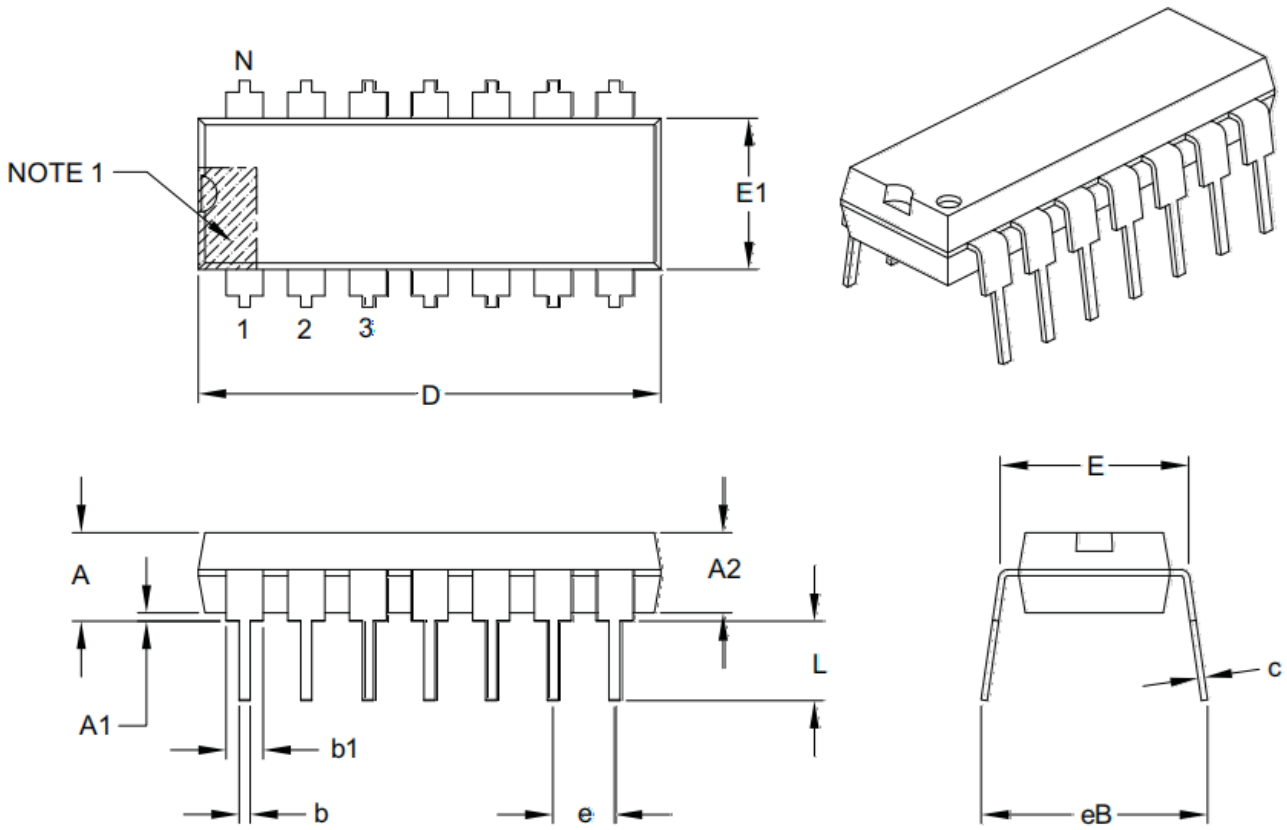
Note **1:** When NPOR is low, the device is held in Reset.

2: TPOR 1 us typical.

3: TVLOW 2.7 us typical.

Package Details

DIF81F1843DI, 14-Lead Plastic Dual In-Line (P)-300 mil Body [DIP]



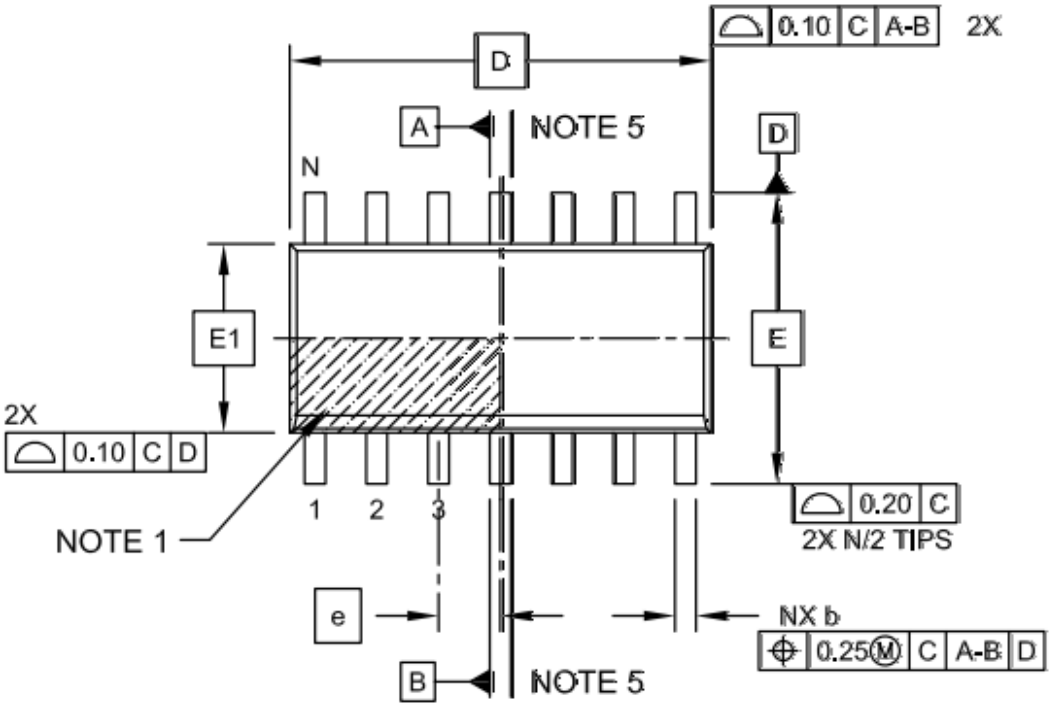
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

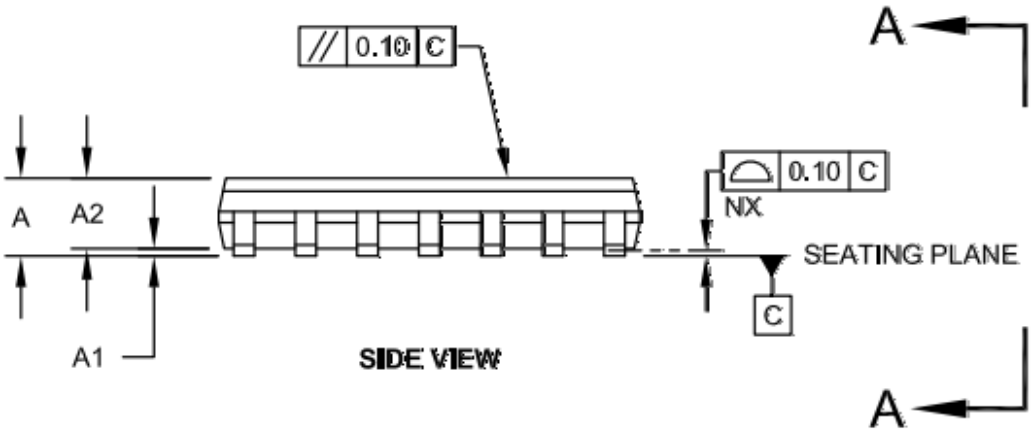
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

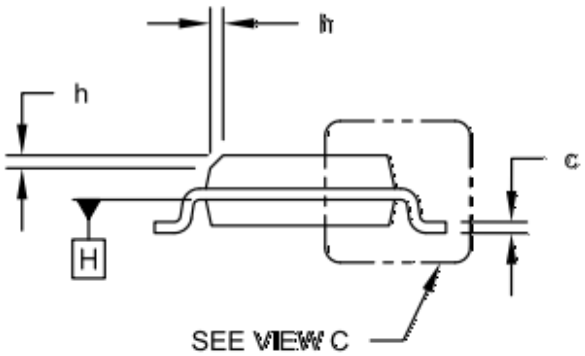
DIF81F1843SI, 14-Lead Plastic Small Outline (SL)-Narrow, 3.90 mm Body [SOIC]



TOP VIEW

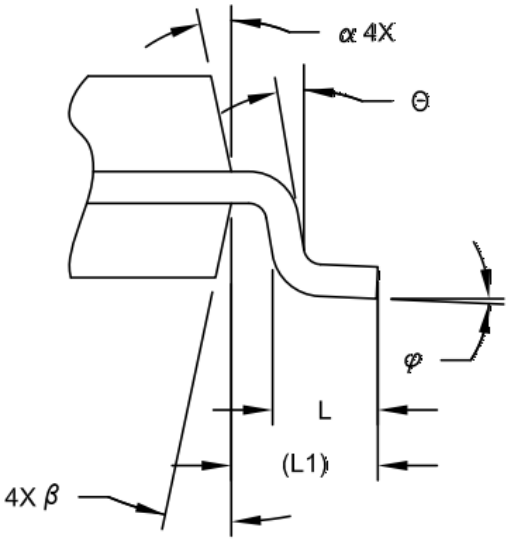


SIDE VIEW

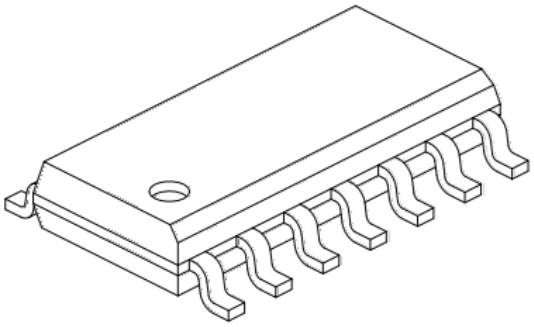


VIEW A-A

DIF81F1843SI, 14-Lead Plastic Small Outline (SL)-Narrow, 3.90 mm Body [SOIC]



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle		0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top		5°	–	15°
Mold Draft Angle Bottom		5°	–	15°

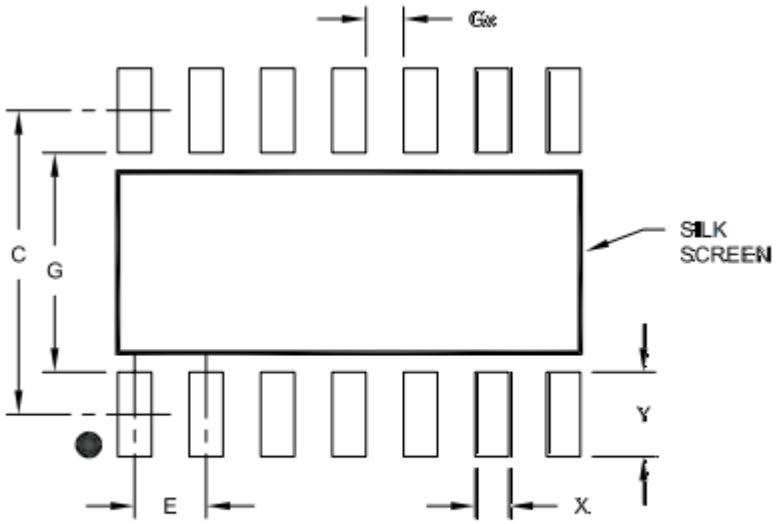
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F1843SI, 14-Lead Plastic Small Outline (SL)-Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

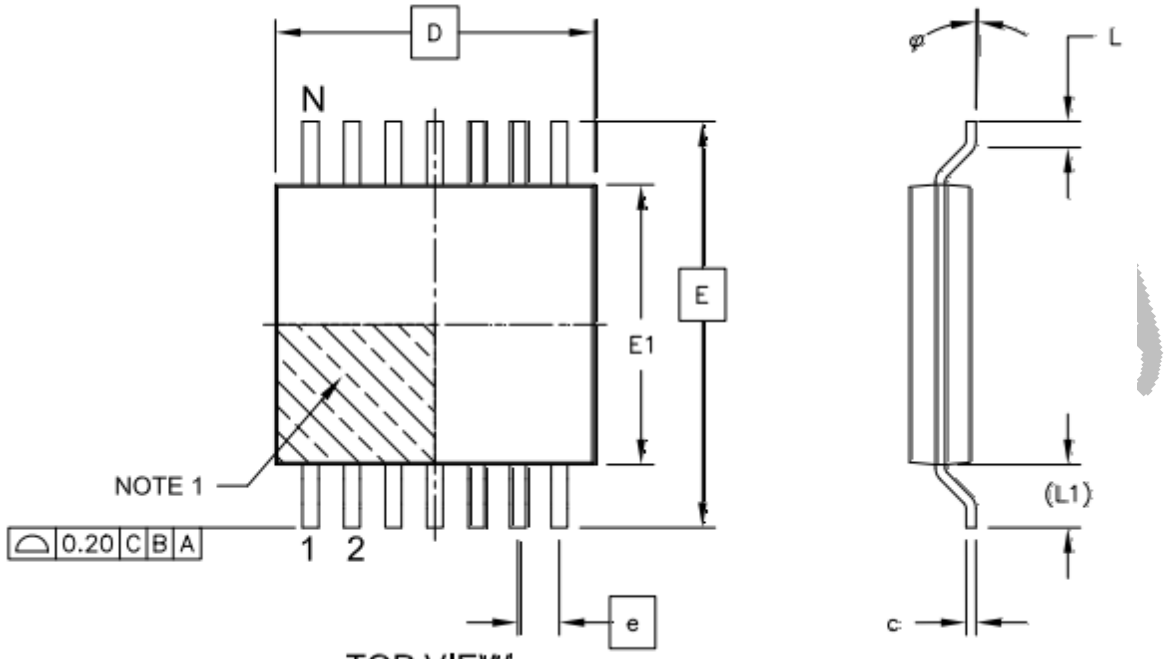
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X1			0.60
Contact Pad Length	Y1			1.55
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

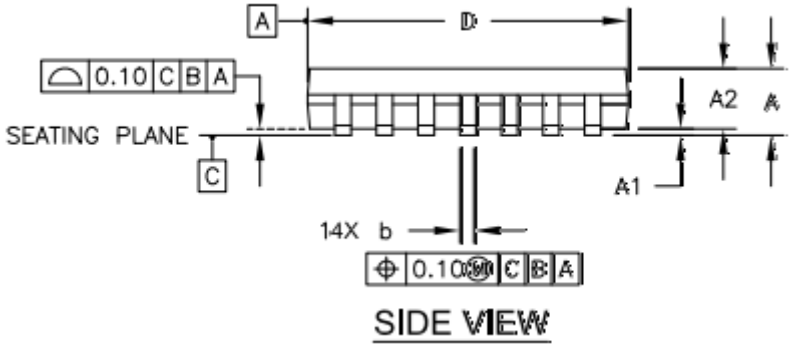
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

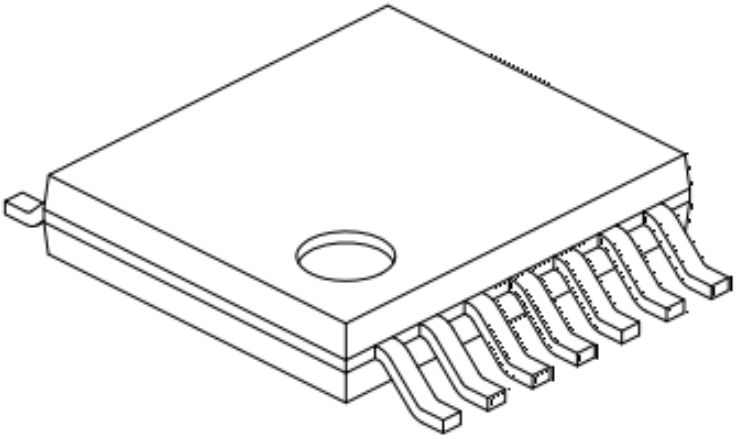
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF81F1843TI, 14 Lead Plastic Thin Shrink Small Outline(ST)-4.4mm Body[TSSOP]





DIF81F1843TI, 14-Lead Plastic Thin Shrink Small Outline(ST) - 4.4mm Body[TSSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff §	A1	0.05	-	0.15
Overall Width	E		6.40BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

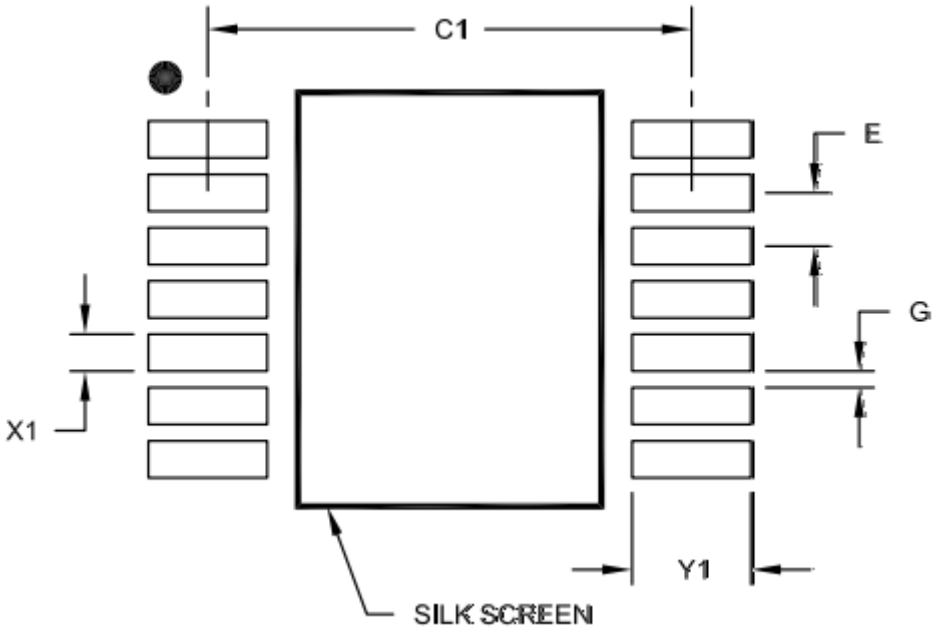
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

DIF81F1843TI, 14Lead Plastic Thin Shrink Small Outline(ST)-4.4mm Body[TSSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width(X14)	X1			0.60
Contact Pad Length(X14)	Y1			1.55
Distance Between Pads	G	0.2		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.