Difmicro Technolog

DIF80F647

Datasheet

Content

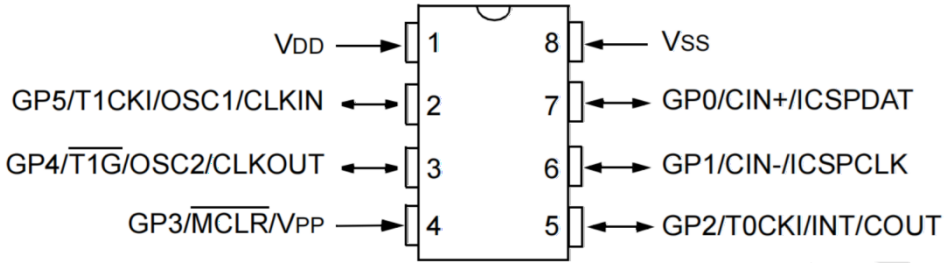
DIF80F647 Performance profile

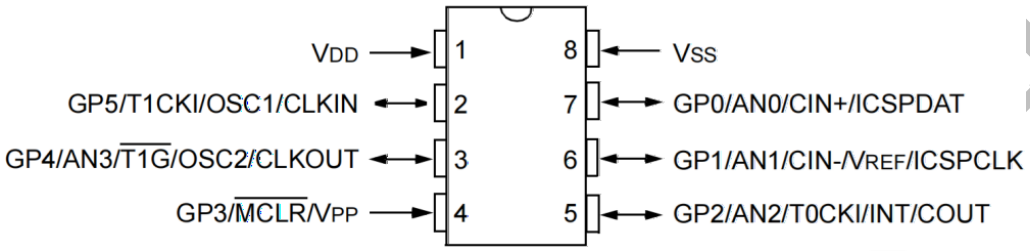
- **Special Microcontroller Features:**
  - High performance, low power 8-bit microprocessor
  - High-performance RISC architecture
  - Only 35 instructions
    - All instructions except jump instructions are single-cycle
  - Operating speed:
    - DC – 20 MHz oscillator/clock input
    - DC – 200 ns instruction cycle
  - Interrupt capability
  - 8-level deep hardware stack
  - Direct, Indirect and Relative Addressing modes
- **Special single chip microcomputer function**
  - Internal and External Oscillator Options
    - Precision Internal 4 MHz oscillator factory calibrated to ±1%
    - External Oscillator support for crystals and resonators
    - 5 us wake-up from Sleep, 3.0V, typical
    - Power-Saving Sleep mode
  - Wide operating voltage range (2.0V-5.5V)
  - Industrial and Extended Temperature range
  - Power-on Reset (POR)
  - Power-up Timer (PWRT) and Oscillator Start-up
  - Timer (OST)
  - Brown-out Reset (BOR) with software control
  - option
  - Enhanced low-current Watchdog Timer (WDT)
  - with on-chip oscillator (software selectable
  - nominal 268 seconds with full prescaler) with
  - software enable
  - Multiplexed Master Clear with pull-up/input pin
  - Programmable code protection
    - 100,000 write Flash endurance
    - 1,000,000 write EEPROM endurance
    - Flash/Data EEPROM retention: > 40 years
- **Low-Power Features**
  - Standby Current:
    - 1nA @ 2.0V, typical
  - Operating Current:
    - 8.5μA @ 32 kHz, 2.0V, typical
    - 100μA @ 1 MHz, 2.0V, typical
  - Watchdog Timer Current:
    - 300nA @ 2.0V, typical
  - Timer1 Oscillator Current:
    - 4 μA @ 32 kHz, 2.0V, typical

- **Peripheral Features**
  - 6 I/O Pins with Individual Direction Control
  - High Current Sink/Source for Direct LED Drive
  - Analog Comparator module with:
    - One analog comparator
    - Programmable on-chip comparator voltage
    - reference (CVREF) module
    - Programmable input multiplexing from device
    - inputs
    - Comparator output is externally accessible
  - Analog-to-Digital Converter module (DIF80F647):
    - 10-bit resolution
    - Programmable 4-channel input
    - Voltage reference input
  - Timer0: 8-Bit Timer/Counter with 8-Bit
  - Programmable Prescaler
  - Enhanced Timer1:
    - 16-bit timer/counter with prescaler
    - External Gate Input mode
    - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
  - In-Circuit Serial Programming (ICSP) viatwo pins

DIF80F647 Pin configuration

DIF80F647 is available in two package forms, DIP and SOP, corresponding to DIF80F647DI(8-pin DIP) and DIF80F647SI(8-pin SOP) respectively





CPU CORE

Structural review

Figure 1 shows the block diagram of the DIF80F647 device.

Table 1 shows the pin arrangement instructions.

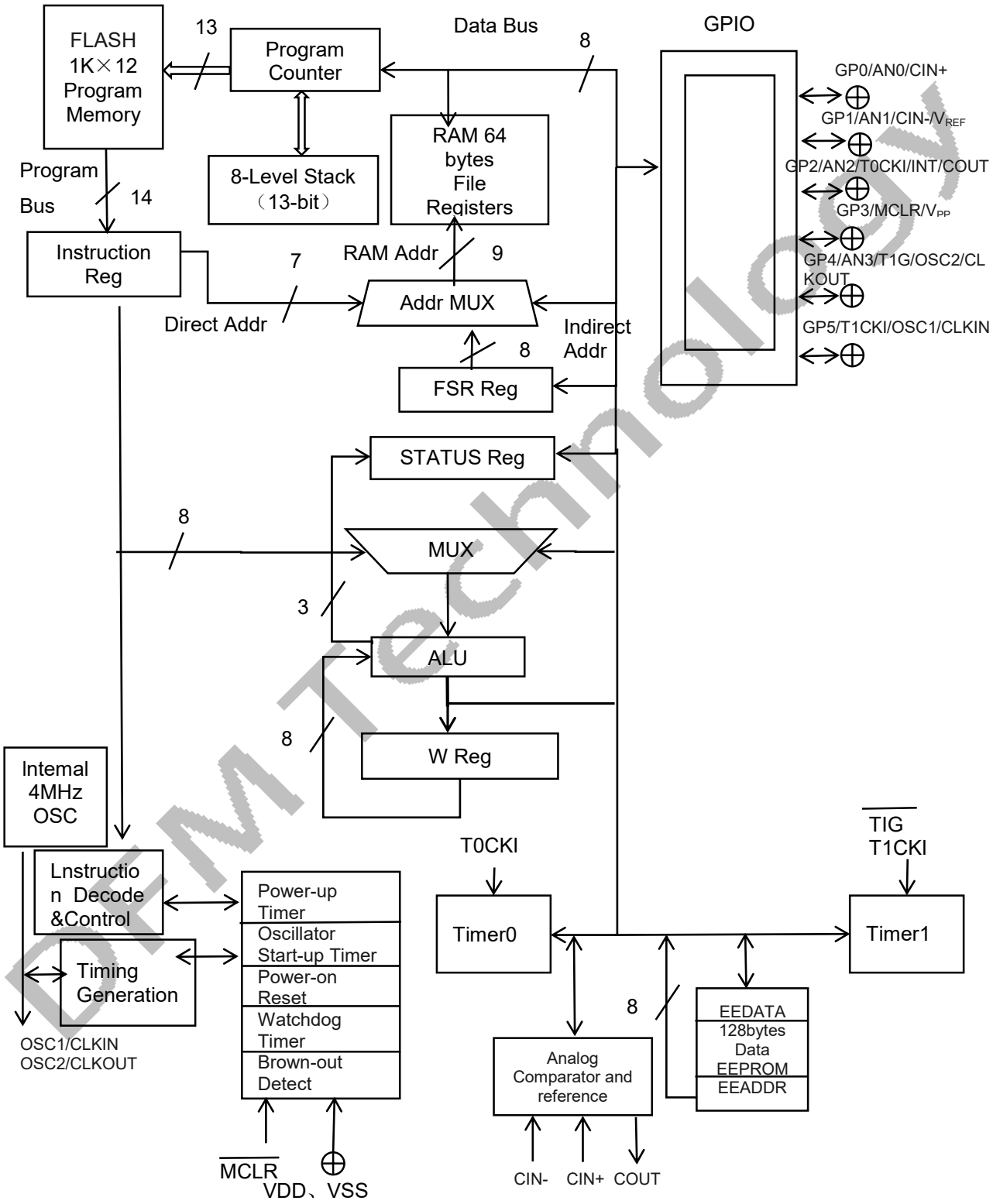


Figure 1.DIF80F647BLOCK DIAGRAM

Table 1.DIF80F647 Pin arrangement instructions

Name	Function	Input Type	Output Type	Description
GP0/AN0/CIN+ /ICSPDAT	GP0	TTL	CMOS	Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	AN0	AN		A/D Channel 0 input
	CIN+	AN		Comparator input
	ICSPDAT	TTL	CMOS	Serial programming I/O
GP1/AN1/CIN-/VREF / ICSPCLK	GP1	TTL	CMOS	Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	AN1	AN		A/D Channel 1 input
	CIN-	AN		Comparator input
	VREF	AN		External voltage reference
	ICSPCLK	ST		Serial programming clock
GP2/AN2/T0CKI/INT /COUT	GP2	ST	CMOS	Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	AN2	AN		A/D Channel 2 input
	T0CKI	ST		TMR0 clock input
	INT	ST		External interrupt
	COUT		CMOS	Comparator output
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL		Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	$\overline{\text{MCLR}}$	ST		Master Clear
	VPP	HV		Programming voltage
GP4/AN3/$\overline{\text{T1G}}$/OSC2 /CLKOUT	GP4	TTL	CMOS	Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	AN3	AN		A/D Channel 3 input
	$\overline{\text{T1G}}$	ST		TMR1 gate
	OSC2		XTAL	Crystal/resonator
	CLKOUT		CMOS	FOSC/4 output
GP5/T1CKI/OSC1 /CLKIN	GP5	TTL	CMOS	Bidirectional I/Ow/programmable pull-up and Interrupt-on-change
	T1CKI	ST		TMR1 clock
	OSC1	XTAL		Crystal/resonator
	CLKIN	ST		External clock input/RC oscillator connection
VSS	VSS	Power		Ground reference
VDD	VDD	Power		Positive supply

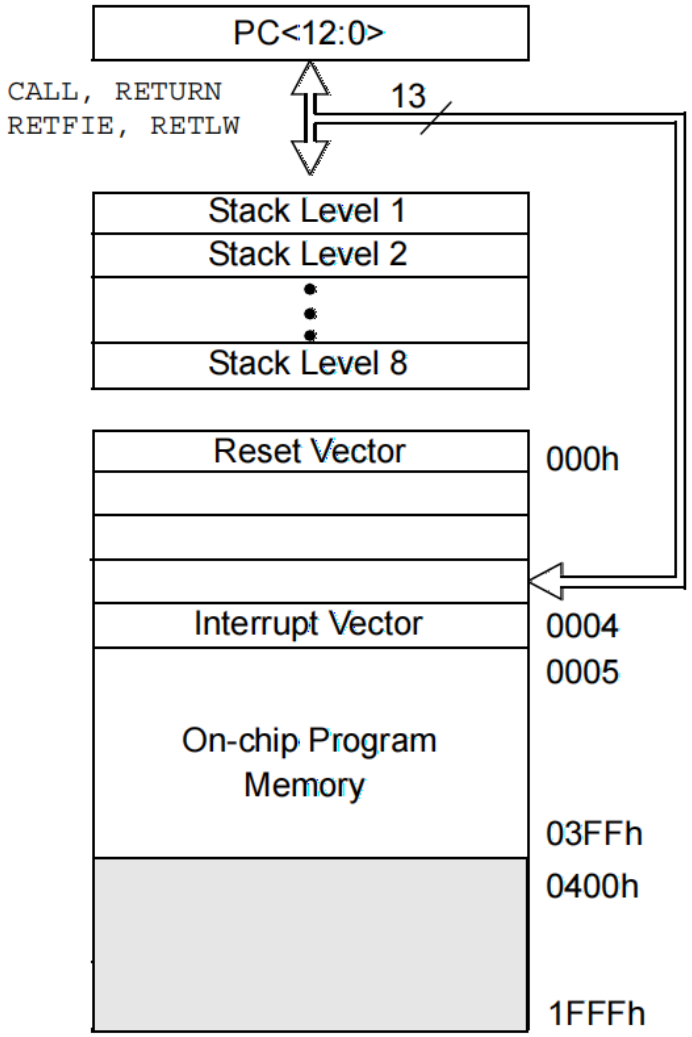
Legend： Shade = DIF80F647 only

TTL = TTL input buffer, ST = Schmitt Trigger input buffer

DIF80F647 MEMORY ORGANIZATION

Program Memory Organization

The DIF80F647 device has a 13-bit program counter that can be used to address 8K x 14 program memory space. For the DIF80F647 device, only the first 1K x 14 (0000h-03FFh) memory unit is physically implemented. Accessing a storage unit that exceeds the above limits creates a loop in the first 1K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2).



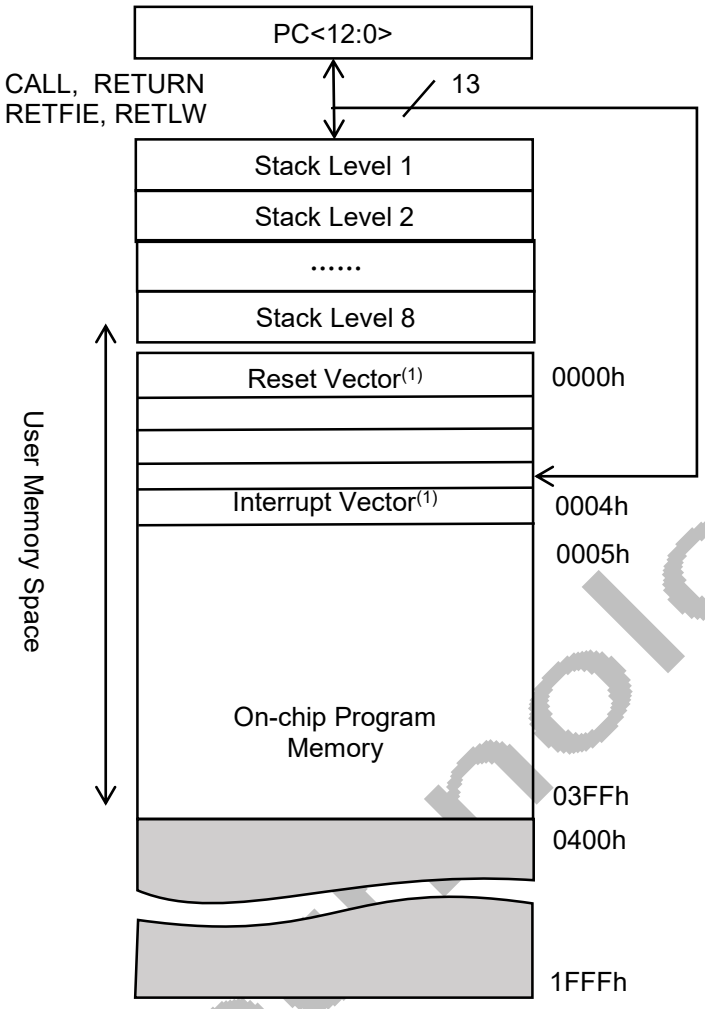


Figure 2.DIF80F647 Program memory map and stack

Data Memory Organization

The data memory is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns ‘0’ when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

Note: The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as ‘0’s.

GENERAL PURPOSE REGISTER FILE

The organization of the general register data in the DIF80F647 device is 64 x 8. Each Register can be accessed "directly" or "indirectly" via a File Select Register (FSR).

SPECIAL FUNCTION REGISTERS

Special function registers are registers that CPU and peripheral functions use to control devices to perform desired operations. These registers are static RAM.

Special function registers can be divided into two categories: kernel and peripherals.

Bank 0		Bank 1	
Indirect Addr TMR0	00h	Indirect Addr	80h
PCL	01h	OPTION REG	81h
STATUS	02h	PCL	82h
FSR	03h	FSR	83h
GPIO	04h	TRISIO	84h
	05h		85h
	06h		86h
	07h		87h
	08h		88h
PCLATH	09h	PCLATH	89h
INTCON	0Ah	INTCON	8Ah
PIR1	0Bh	PIE1	8Bh
	0Ch		8Ch
TMR1L	0Dh	PCON	8Dh
TMR1H	0Eh		8Eh
T1CON	0Fh	OSCCAL	8Fh
	10h	ANSEL	90h
	11h		91h
	12h		92h
	13h		93h
	14h		94h
	15h	WPU	95h
	16h	IOC	96h
	17h		97h
	18h		98h
	19h	VRCON	99h
CMCON	1Ah	EEDAT	9Ah
	1Bh	EEADR	9Bh
	1Ch	EECON1	9Ch
	1Dh	EECON2	9Dh
	1Eh	ADRESL	9Eh
	1Fh	ADCON1	9Fh
ADRESH		Accesses 20h-5Fh	A0h
ADCON0	20h		DFh
GENERAL PURPOSE REGISTER 64 Bytes	5Fh		

Figure 3.DIF80F647 Data memory mapping

Table 2. Summary of special function registers

Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Value on POR、 BOD
Bank 0										
00h	INDF(1)	Addressing this Location uses Contents of FSR to Address Data Memory								0000 0000
01h	TMR0	Timer0 Module's Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	IRP(2)	RP1(2)	RP0	TO	PD	Z	DC	C	0001 1xxx
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
05h	GPIO	—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	--xx xxxx
06h	—	Unimplemented								—
07h	—	Unimplemented								—
08h	—	Unimplemented								—
09h	—	Unimplemented								—
0Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0
0Dh	—	Unimplemented								—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit Timer1								xxxx xxxx
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit Timer1								xxxx xxxx
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000
11h	—	Unimplemented								—
12h	—	Unimplemented								—
13h	—	Unimplemented								—
14h	—	Unimplemented								—
15h	—	Unimplemented								—
16h	—	Unimplemented								—
17h	—	Unimplemented								—
18h	—	Unimplemented								—
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000
1Ah	—	Unimplemented								—
1Bh	—	Unimplemented								—
1Ch	—	Unimplemented								—
1Dh	—	Unimplemented								—
1Eh	ADRESH(3)	Most Significant 8 bits of the Left Shifted A/D Result or 2 bits of the Right Shifted Result								xxxx xxxx
1Fh	ADCON0(3)	ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON	00-- 0000

Legend: - = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition

shaded = unimplemented

Note: **1:** This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

Table 3. Summary of special function registers

Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Value on POR、 BOD
Bank 1										
80h	INDF(1)	Addressing this Location uses Contents of FSR to Address Data Memory								0000 0000
81h	OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	IRP(2)	RP1(2)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111
86h	—	Unimplemented								—
87h	—	Unimplemented								—
88h	—	Unimplemented								—
89h	—	Unimplemented								—
8Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0
8Dh	—	Unimplemented								—
8Eh	PCON	—	—	—	—	—	—	POR	BOD	---- --0x
8Fh	—	Unimplemented								—
90h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--
91h	—	Unimplemented								—
92h	—	Unimplemented								—
93h	—	Unimplemented								—
94h	—	Unimplemented								—
95h	WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000
97h	—	Unimplemented								—
98h	—	Unimplemented								—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000
9Ah	EEDATA	Data EEPROM Data Register								0000 0000
9Bh	EEADR	—	Data EEPROM Address Register							-000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000
9Dh	EECON2(1)	EEPROM Control Register 2								---- ----
9Eh	ADRESL(3)	Least Significant 2 bits of the Left Shifted A/D Result of 8 bits or the Right Shifted Result								xxxx xxxx
9Fh	ANSEL(3)	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111

Legend: - = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition
shaded = unimplemented

Note: **1:** This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias..... -40 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on VDD with respect to VSS ..... -0.3 to +6.5V

Voltage on MCLR with respect to Vss .....-0.3 to +13.5V

Voltage on all other pins with respect to VSS ..... -0.3V to (VDD + 0.3V)

Total power dissipation(1) 800mW

Maximum current out of VSS pin 300mA

Maximum current into VDD pin 250mA

Input clamp current, IIK (VI < 0 or VI >VDD).....20mA

Output clamp current, IOK (Vo < 0 or Vo >VDD).....20mA

Maximum output current sunk by any I/O pin..... 25mA

Maximum output current sourced by any I/O pin 25mA

Maximum current sunk by all GPIO 125mA

Maximum current sourced all GPIO..... 125mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to V_{SS}.

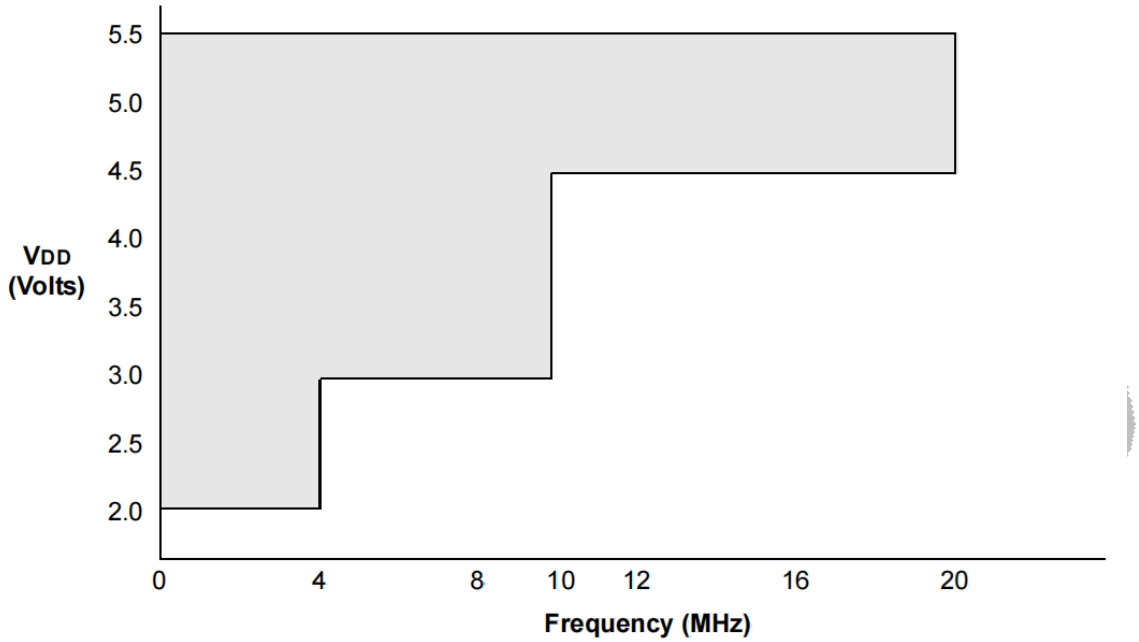


图 **1.**DIF80F647 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH, -40° C≤TA≤+125° C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

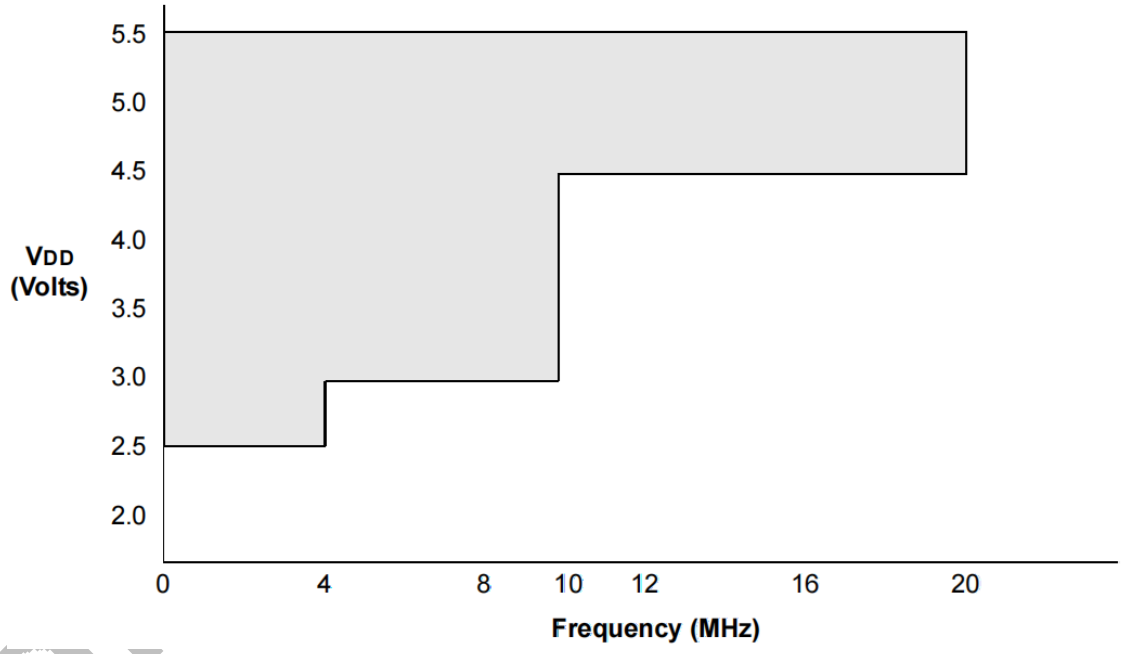


Figure 2.DIF80F647 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH, -40° C≤TA≤ +125° C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

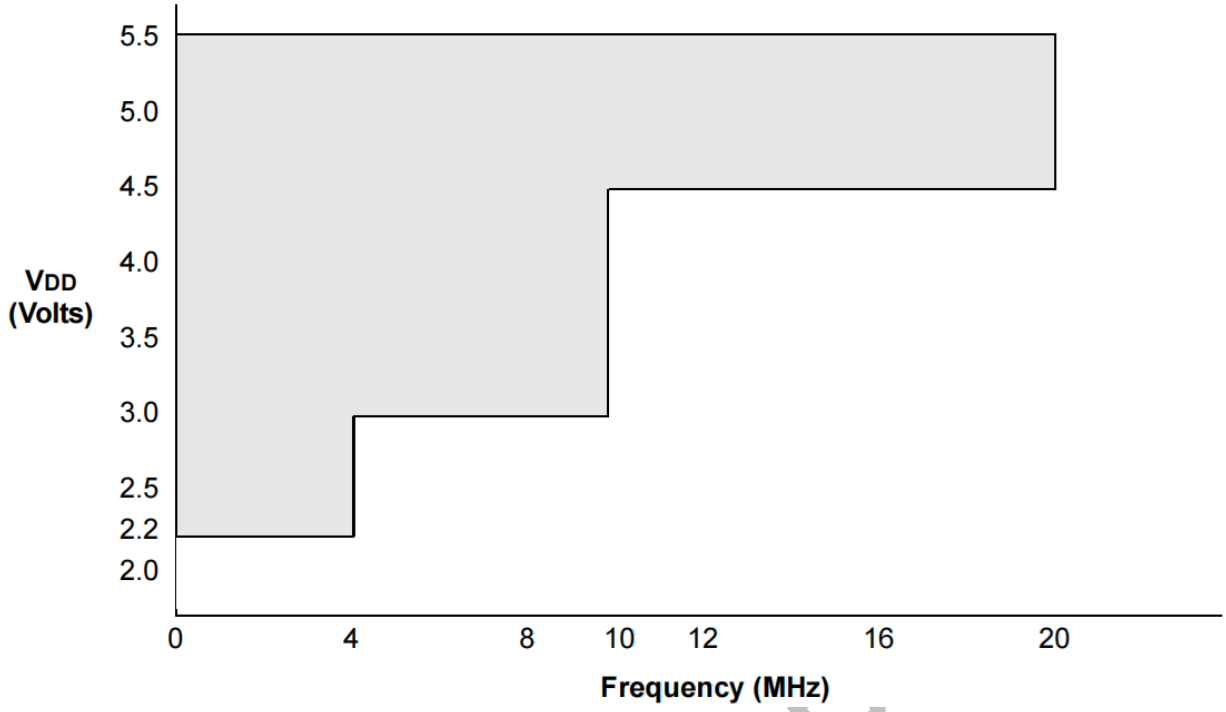
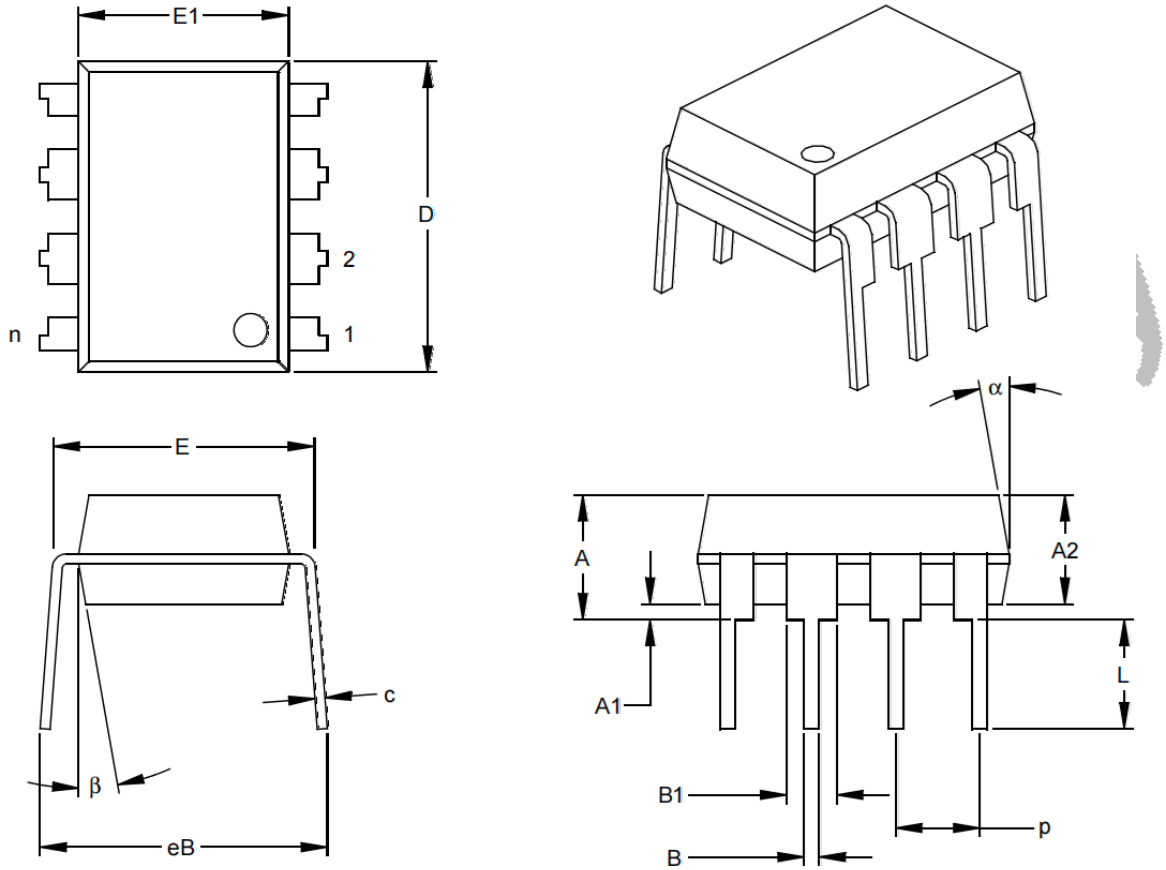


图 3.DIF80F647WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH, 0° C ≤ TA ≤ +125° C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

Package Details

8-Lead Plastic Dual In-Line (D), 300 mil(DIP) Corresponding model is DIF80F647DI

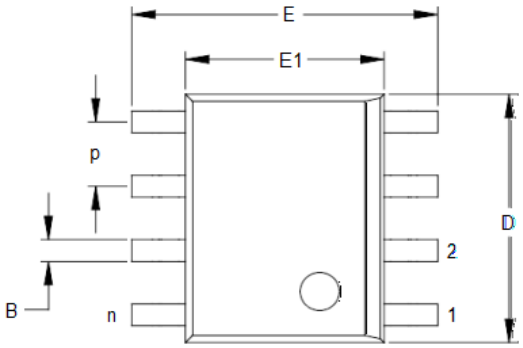


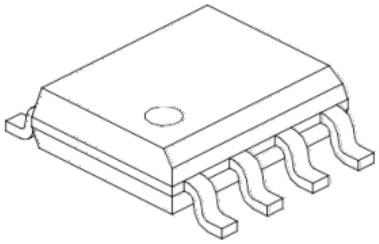
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	—	—	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	—	—
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	—	—	.430

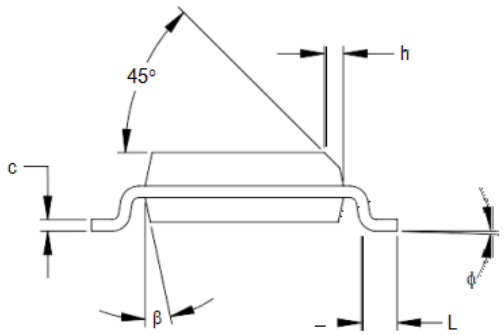
Notes：

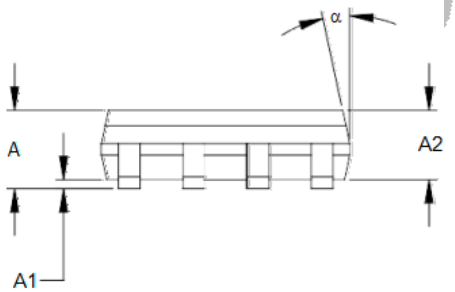
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC:Basic Dimension.Theoretically exact value shown without tolerances.

8-Pin plastic encapsulation small package(S)-Narrow, 3.9mm(SOP), Corresponding model is DIF80F647SI









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.1.27 BSC	
Over Height	A	—	—	1.75
Molded Package Thickness	A2	1.25	—	—
Standoff §	A1	0.10	—	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer(Optional)	h	0.25	—	0.50
Foot Length	L	0.40	—	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	—	8°
Lead Thickness	c	0.17	—	0.25
Lead Width	b	0.31	—	0.51
Mold Draft Angle Top	α	5°	—	15°
Mold Draft Angle Bottom	β	5°	—	15°

Notes：

5. Pin 1 visual index feature may vary, but must be located within the hatched area.
6. § Significant Characteristic
7. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
8. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.