Difmicro Technolog

DIF80F526

Datasheet

Content

DIF80F526 Product characteristics

- **8-Pin Flash-Based, 8-Bit**
- **High-Performance RISC CPU:**

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions Except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- 2-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 8 Special Function Hardware Registers
  - Operating Speed:
  - DC – 4 MHz clock input
  - DC – 1000 ns instruction cycle

- **Special Microcontroller Features:**

- 4 MHz Precision Internal Oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming (ICSP)
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed MCLR Input Pin
- Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-Wp from Sleep on Pin Change
- Selectable Oscillator Options:
  - INTRC: 4 MHz precision Internal oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - LP: Power-saving, low-frequency crystal

- **Low-Power Features/CMOS Technology:**

- Operating Current:
  - < 175 A @ 2V, 4 MHz, typical
- Standby Current:
  - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
  - 100,000 Flash endurance
  - > 40 years retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
  - Industrial: -40℃ to +85℃
  - Extended: -40℃ to +125℃

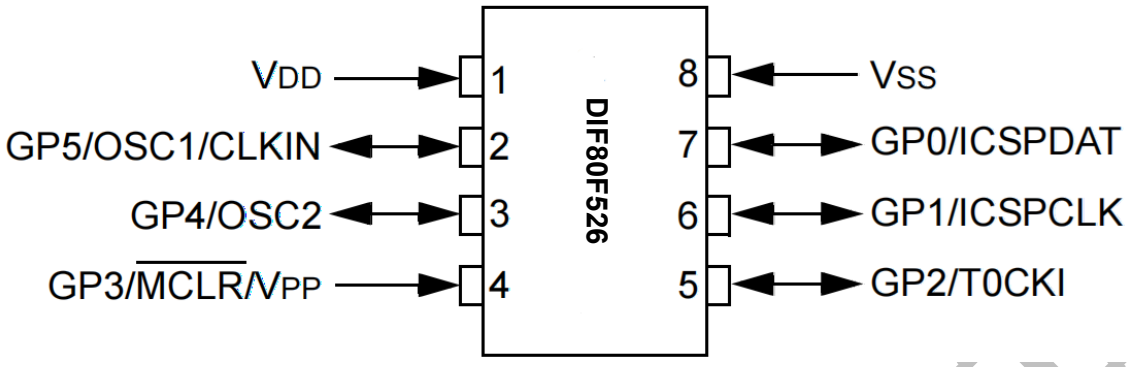
Peripheral Features (DIF80F526):

- 6 I/O Pins:
  - 5 I/O pins with individual direction control
  - 1 input only pin
  - High current sink/source for direct LED drive
  - Wake-on-change
  - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Device	Program Memory	Data Memory	I/O	Timers 8-bit
	Flash (words)	SRAM (bytes)		
DIF80F526	512	25	6	1

Pin Diagrams

DIF80F526DI(8-pin DIP),and DIF80F526SI(8-pin SOIC)



CPU Kernel

DEVICE OVERVIEW

The high performance of the DIF80F526 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the DIF80F526 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz, 1us @ 4 MHz) except for program branches.

Table 1.DIF80F526 MEMORY

Device	Memory	
	Program	Data
DIF80F526	512 x 12	25 x 8

The DIF80F526 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The DIF80F526/ 16F505 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the ZDIF80F526 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The DIF80F526 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, sub- traction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

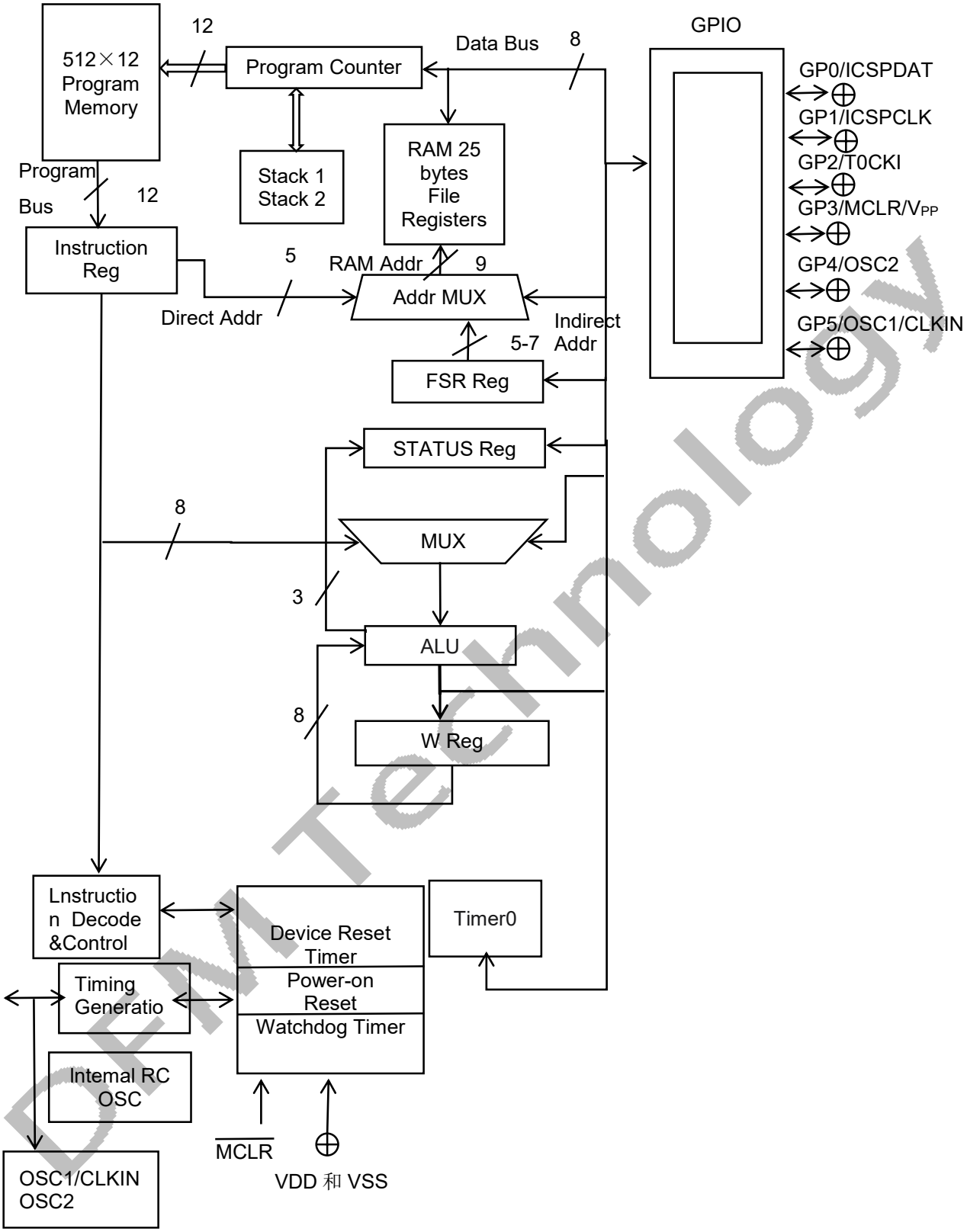


Figure 1.DIF80F526 BLOCK DIAGRAM

Table 2.DIF80F526 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/ICSPDAT	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming data pin.
GP1/ICSPCLK	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.
GP2/T0CKI	GP2	TTL	CMOS	Bidirectional I/O pin.
	T0CKI	ST	—	Clock input to TMR0.
GP3/MCLR/VPP	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	MCLR	ST	—	Master Clear (Reset). When configured as MCLR, this pin is an active-low Reset to the device. Voltage on MCLR/VPP must not exceed VDD during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as MCLR.
	VPP	HV	—	Programming voltage input.
GP4/OSC2	GP4	TTL	CMOS	Bidirectional I/O pin.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT and LP modes only, GPIO in other modes).
GP5/OSC1/CLKIN	GP5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Oscillator crystal input.
	CLKIN	ST	—	External clock source input.
VDD	VDD	—	P	Positive supply for logic and I/O pins.
VSS	VSS	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4.

Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction.

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

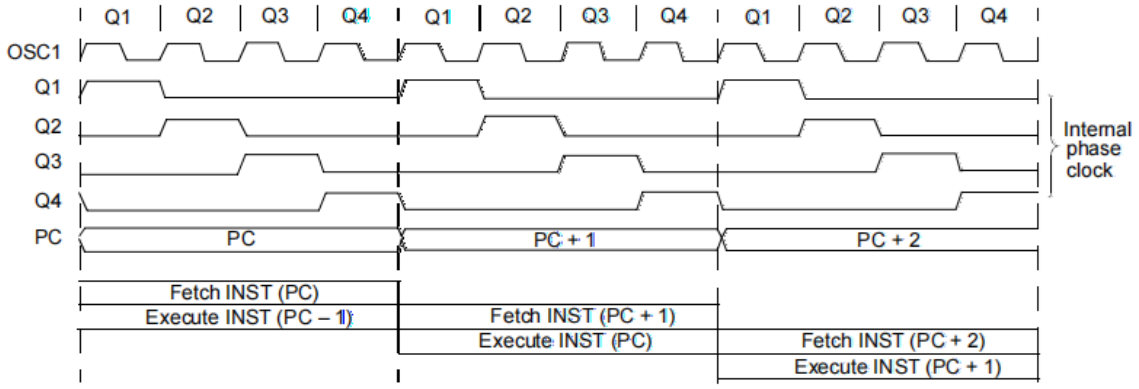
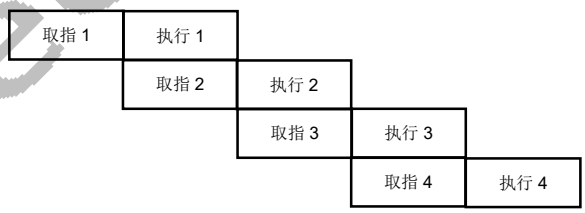


Figure 2.CLOCK/INSTRUCTION CYCLE

EXAMPLE:

```
1.CLRF    02h
2.CLRW
3.CLRF    GPIO
4.BSF     GPIO,BIT1
```



除程序转移指令外，所有指令都是单周期指令。由于程序转移指令将导致一条已取指令从流水线清除，需要重新取指，然后执行指令，所以程序转移指令需要两个周期。

MEMORY ORGANIZATION

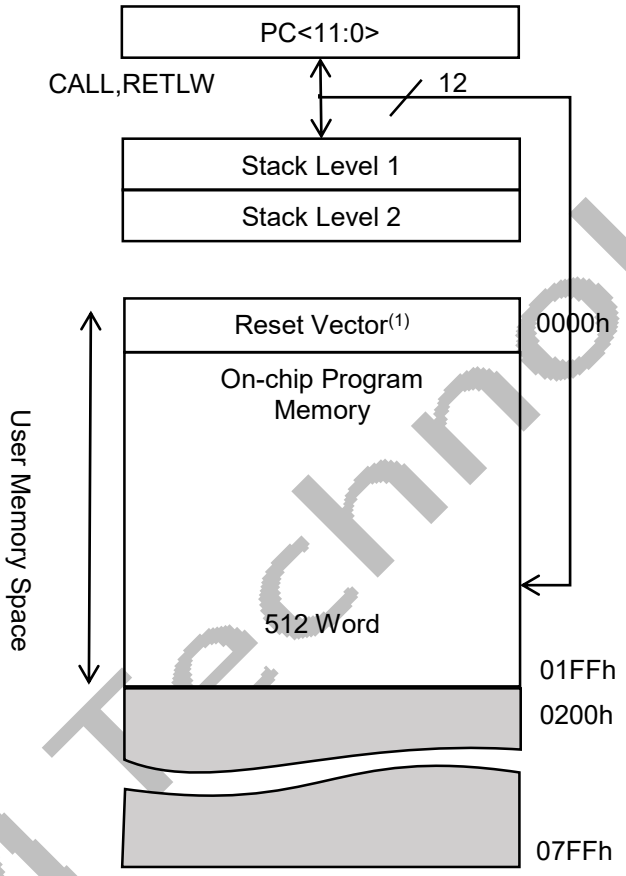
The DIF80F526 memories are organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one STATUS register bit.

Program Memory Organization for the DIF80F526

The DIF80F526 device has a 10-bit Program Counter (PC) and capable of addressing a 2K x 12 program memory space.

Only the first 512 x 12 (0000h-01FFh) for the DIF80F526 are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first.

512 x 12 space (DIF80F526). The effective Reset vector is a 0000h. Location 01FFh(DIF80F526) contain the internal clock oscillator calibration value. This value should never be overwritten.



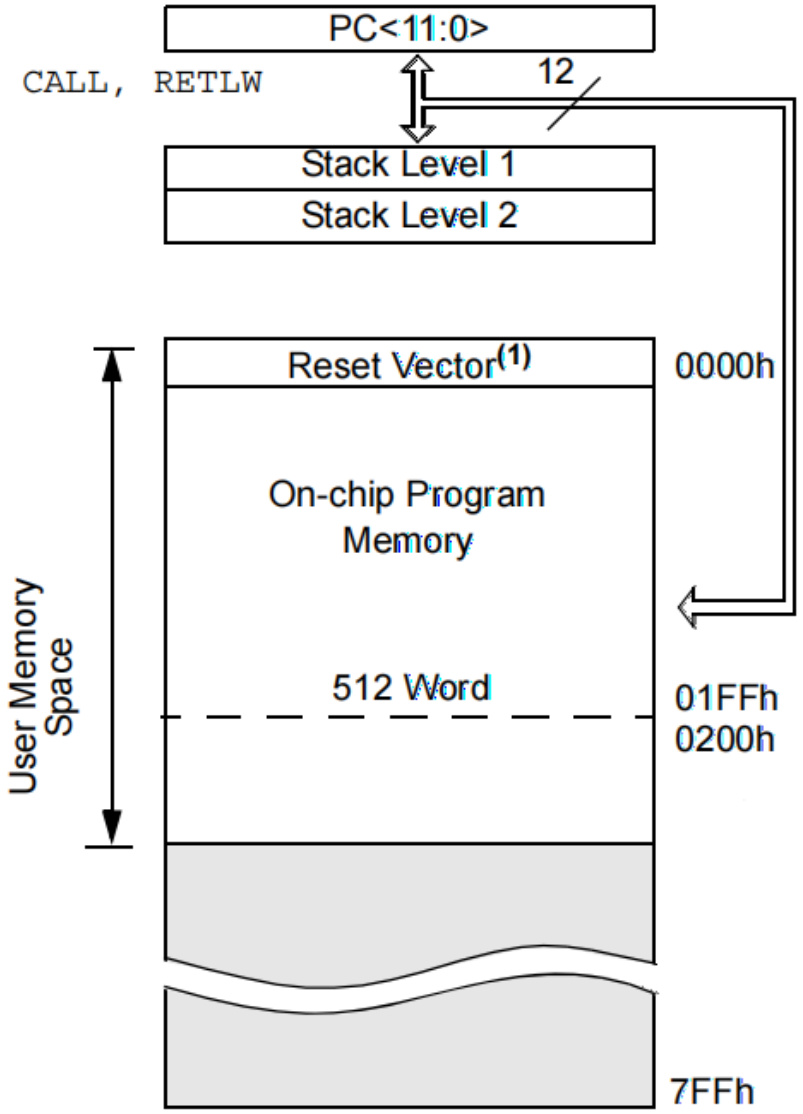


Figure 3.ROGRAM MEMORY MAP AND STACK FOR THE DIF80F526

Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

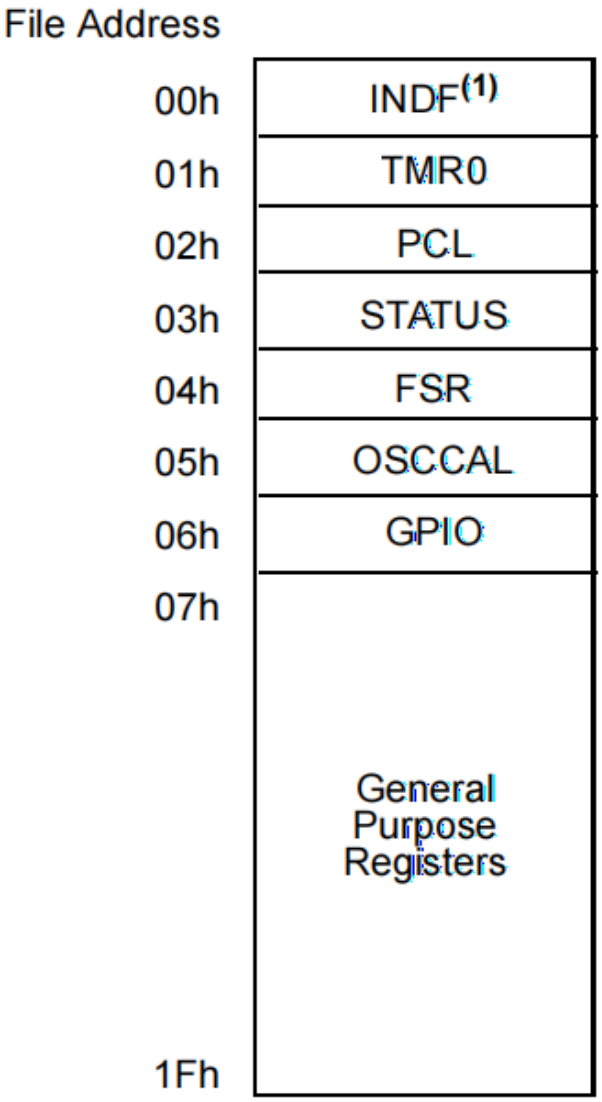
The Special Function Registers include the TMR0 register, the Program Counter (PCL), the STATUS register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the DIF80F526, the register file is composed of 7 Special Function Registers, 9 General Purpose Registers and 16 or 32 General Purpose Registers accessed by banking.

GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register (FSR).



Note 1: Not a physical register.

SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device.

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Table 3.SPECIAL FUNCTION REGISTER (SFR) SUMMARY (DIF80F526)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx
02h(1)	PCL	Low-order 8 bits of PC								1111 1111
03h	STATUS	GPWUF	—	PA0(5)	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0-01 1xxx(3)
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx
04h(4)	FSR	Indirect Data Memory Address Pointer								110x xxxx
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx
N/A	TRISGPIO	—	—	I/O Control Register						--11 1111
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111

Legend: – = unimplemented, read as ‘0’, x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible.

2: Other (NON Power-up) Resets include external Reset through MCLR, Watchdog Timer and wake-up on pin change Reset.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

4: For code compatibility do not use this bit on the DIF80F526.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias..... -40°C to +125°C
Storage temperature..... -65°C to +150°C
Voltage on VDD with respect to VSS.....0 to +6.5V
Voltage on $\overline{MCLR}$ with respect to VSS.....0 to +13.5V
Voltage on all other pins with respect to VSS.....0.3V to (VDD + 0.3V)
Total power dissipation(1).....800 mW
Max. current out of VSS pin.....200 mA
Max. current into VDD pin.....150 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > VDD).....±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > VDD).....±20 mA
Max output current sunk by any I/O pin.....25 mA
Max output current sourced by any I/O pin.....25 mA
Max output current sourced by I/O port.....75 mA
Max output current sunk by I/O port.....75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

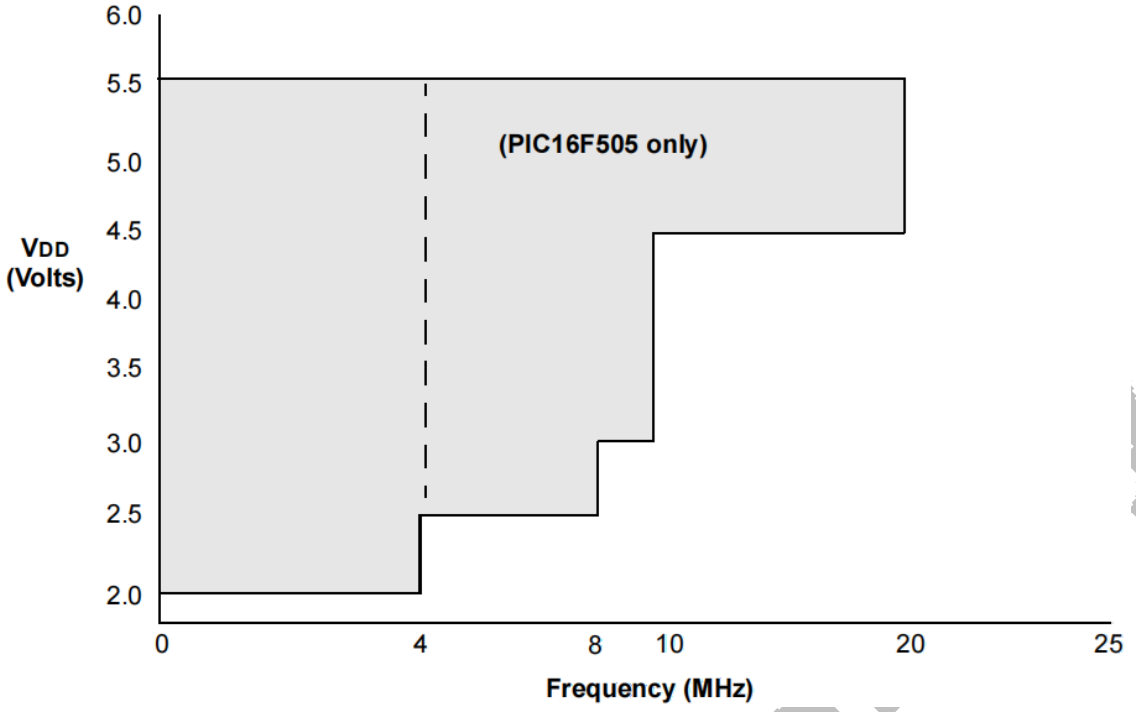


Figure **4.**DIF80F526 VOLTAGE-FREQUENCY GRAPH,-40℃ ≤ TA ≤ +125℃

DC Characteristics: DIF80F526

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See Figure 10-1
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	
D010	IDD	**Supply Current(3,4)**	— —	175 0.625	275 1.1	μA mA	FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V
			— —	500 1.5	650 2.2	μA mA	FOSC = 10 MHz, VDD = 3.0V FOSC = 20 MHz, VDD = 5.0V
			— —	11 38	20 54	μA μA	FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V
D020	IPD	**Power-down Current(5)**	— —	0.1 0.35	1.2 2.4	μA μA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**	— —	1.0 7.0	3.0 16.0	μA μA	VDD = 2.0V VDD = 5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25 C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

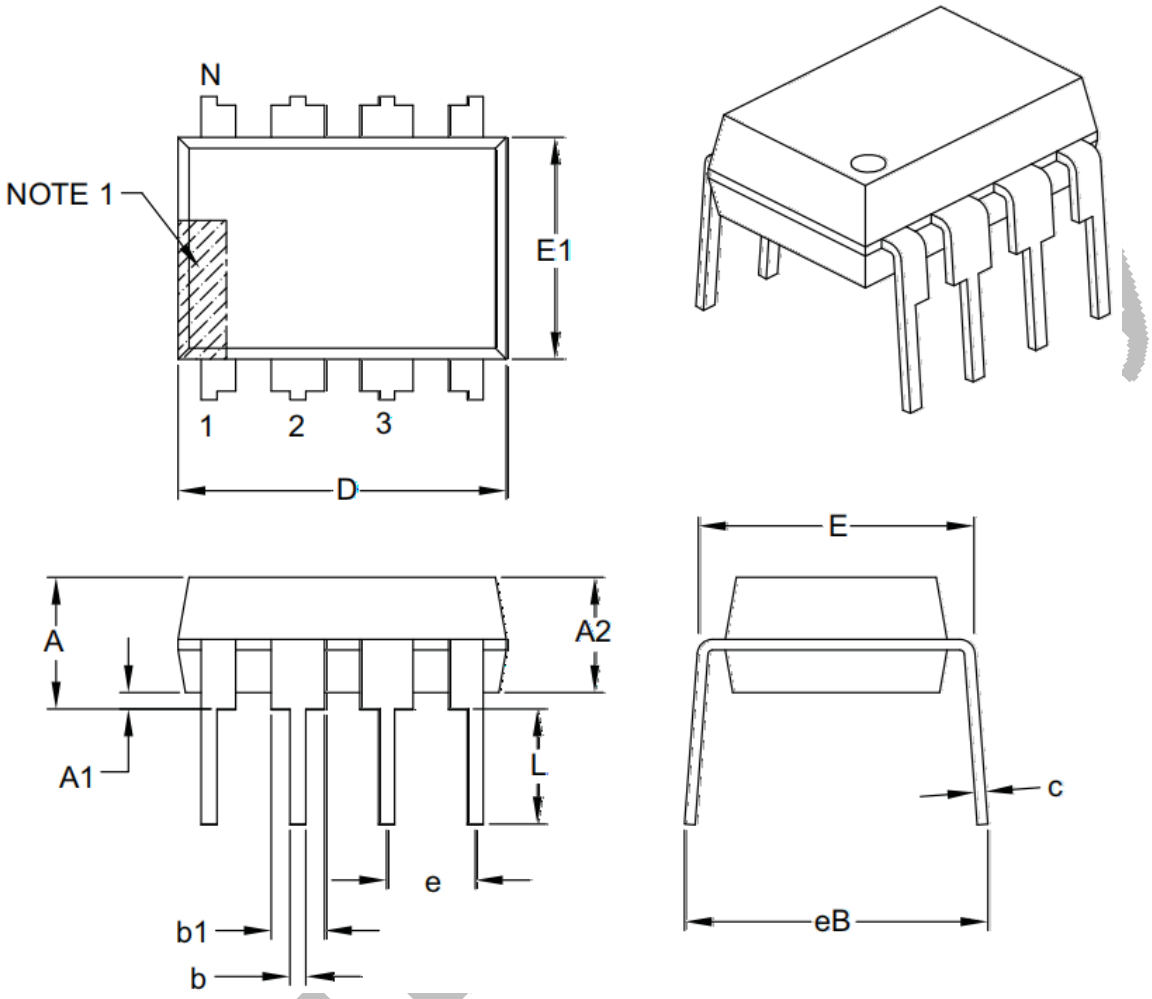
4: The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

Package Details

DIF80F526DI, 8-Lead Plastic Dual In-Line (P) – 300 mil Body [DIP]



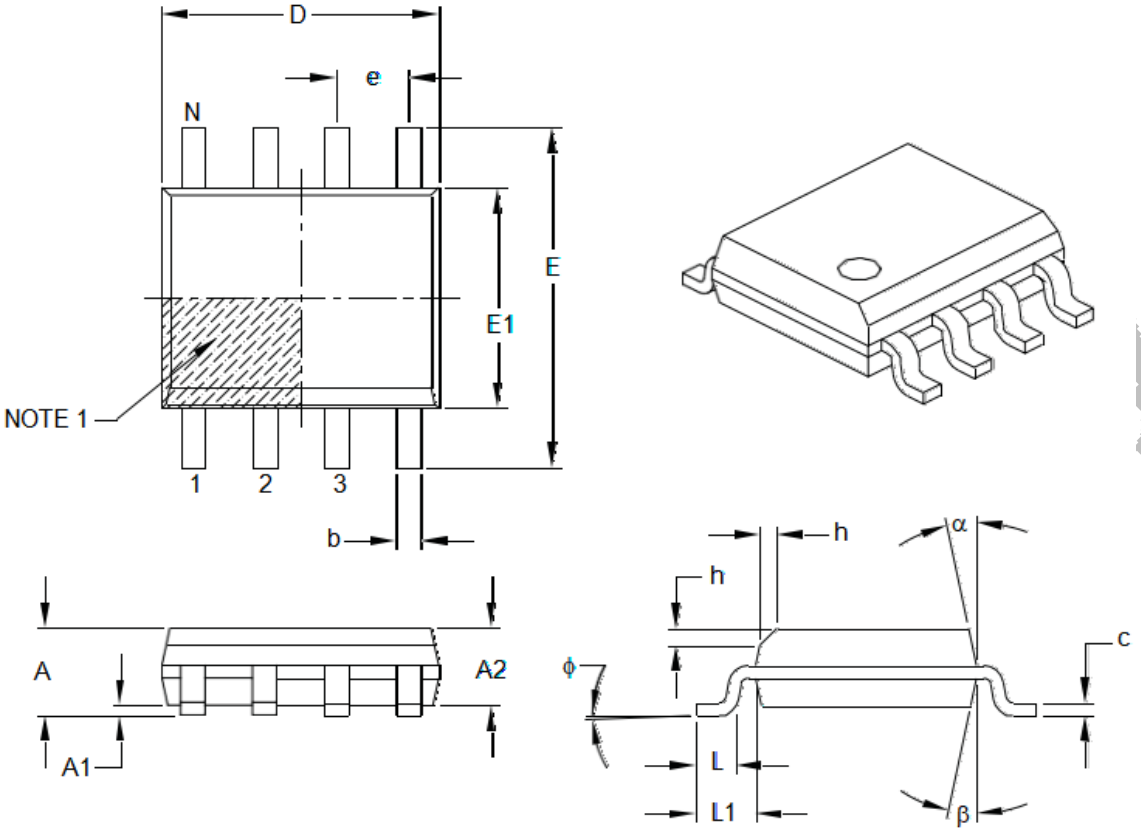
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF80F526SI, 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle		0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top		5°	–	15°
Mold Draft Angle Bottom		5°	–	15°

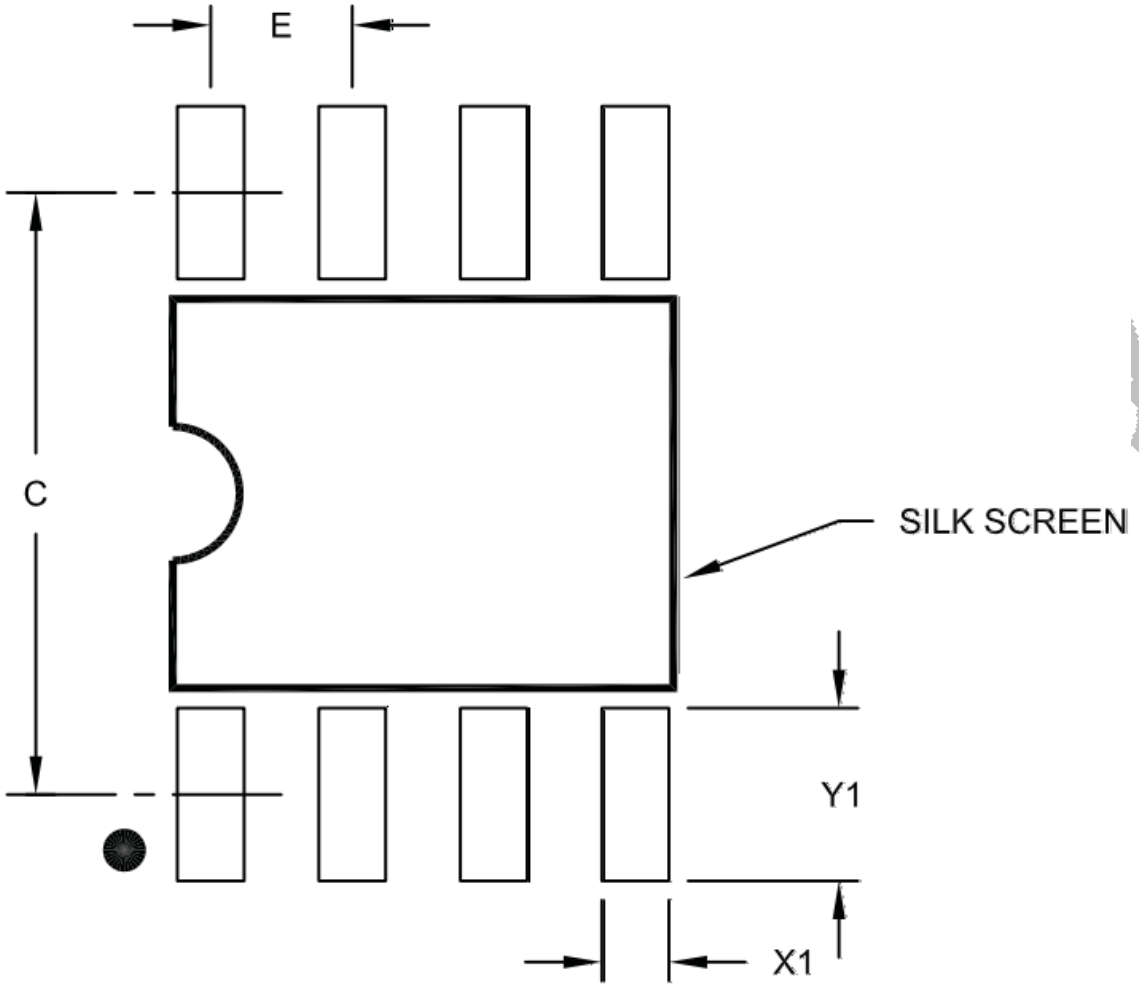
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

8-Lead Plastic Small Outline (SI) – Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width(X8)	X1			0.60
Contact Pad Length(X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.