Difmicro Technolog

DIF80F222

Datasheet

Content

DIF80F222 Product characteristics

High-Performance RISC CPU:

- Only 33 single-word instructions to learn
- All single-cycle instructions except for program branches, which are two-cycle
- 12-bit wide instructions
- 2-level deep hardware stack
- Direct, Indirect and Relative Addressing modes for data and instructions
- 8-bit wide data path
- 8 Special Function Hardware registers
- Operating speed:
  - 4 MHz internal clock
  - 1 us instruction cycle

Special Microcontroller Features:

- 4 MHz precision internal oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming (ICSP)
- In-Circuit Debugging (ICD) support
- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator for reliable operation
- Programmable code protection
- Multiplexed MCLR input pin
- Internal weak pull-ups on I/O pins
- Power-saving Sleep mode
- Wake-up from Sleep on pin change

Low-Power Features/CMOS Technology:

- Operating Current:
  - < 350uA @ 2V, 4 MHz
- Standby Current:
  - 100nA @ 2V, typical
- Low-power, high-speed Flash technology:
  - 100,000 Flash endurance
  - > 40year retention
- Fully static design
- Wide operating voltage range: 2.0V to 5.5V
- Wide temperature range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

- **Peripheral Features:**

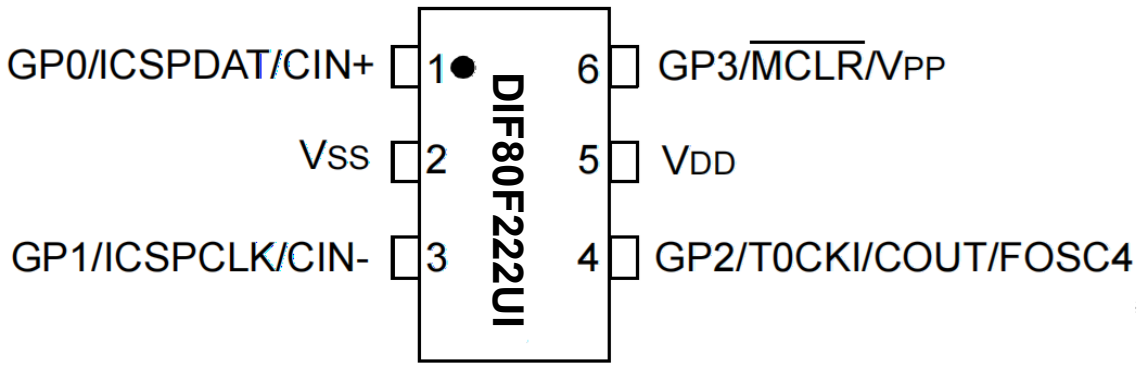
- 4 I/O pins:
  - 3 I/O pins with individual direction control
  - 1 input only pin
  - High current sink/source for direct LED drive
  - Wake-on-change
  - Weak pull-ups
- 8-bit real-time clock/counter (TMR0) with 8-bit programmable prescaler
- 1 Comparator
  - Internal absolute voltage reference
  - Both comparator inputs visible externally
  - Comparator output visible externally

Table 1.DIF80F222

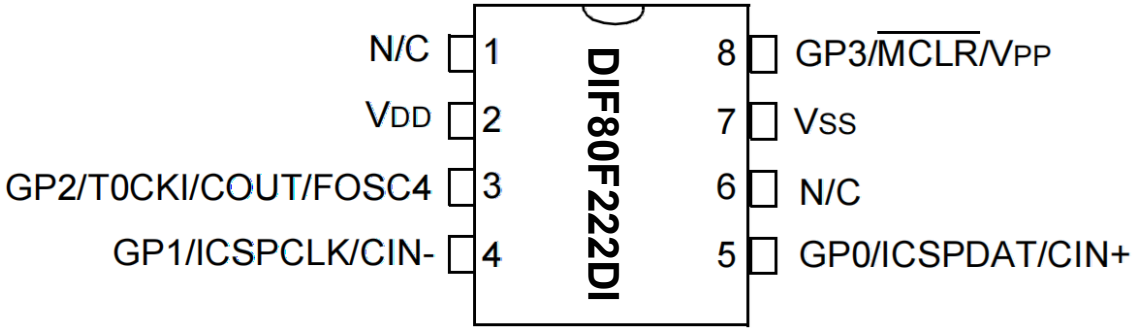
Device	Program Memory Flash (words)	Data Memory SRAM (bytes)	I/O	Timers 8-bit	Comparator
DIF80F222	256	16	4	1	1

Pin Diagrams

DIF80F222UI, 6-pin SOT-23



DIF80F222DI, 8-pin DIP



CPU Kernel

DEVICE OVERVIEW

The high performance of the DIF80F222 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the DIF80F222 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves band- width over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (1us @ 4 MHz) except for program branches.

The table below lists program memory (Flash) and data memory (RAM) for the DIF80F222 devices.

Table 2.DIF80F222 MEMORY

Device	Memory	
	Program	**Data**
DIF80F222	256 x 12	16 x 8

The DIF80F222 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The DIF80F222 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of "special optimal situations" make programming with the DIF80F222 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

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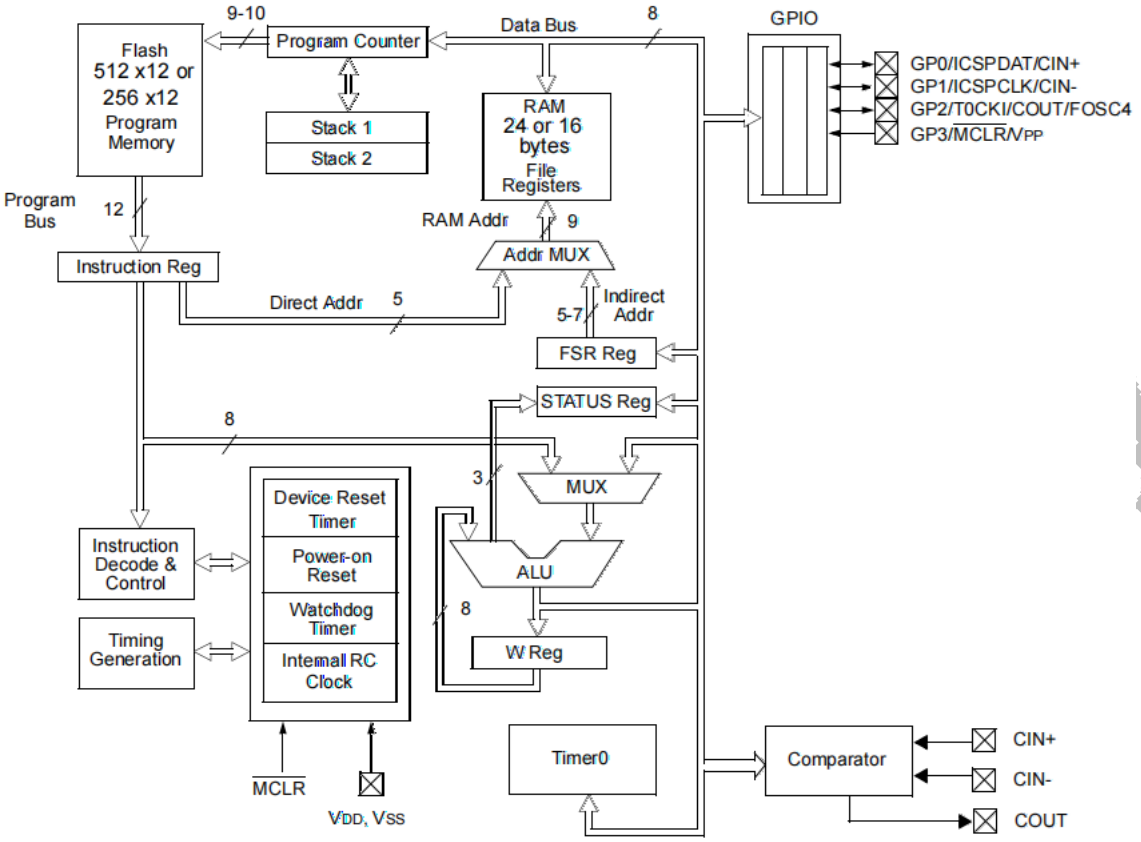

9-10
Program Counter
Data Bus
8
GPIO
Flash
512 x12 or
256 x12
Program
Memory
Stack 1
Stack 2
RAM
24 or 16
bytes
File
Registers
GP0/ICSPDAT/CIN+
GP1/ICSPCLK/CIN-
GP2/T0CKI/COUT/FOSC4
GP3/MCLR/VPP
Program
Bus
12
RAM Addr
9
Addr MUX
Instruction Reg
Direct Addr
5
5-7
Indirect
Addr
FSR Reg
STATUS Reg
8
3
MUX
Device Reset
Timer
Instruction
Decode &
Control
Power-on
Reset
ALU
Watchdog
Timer
Timing
Generation
8
Internal RC
Clock
W Reg
Timer0
Comparator
CIN+
CIN-
COUT
MCLR
VDD, VSS

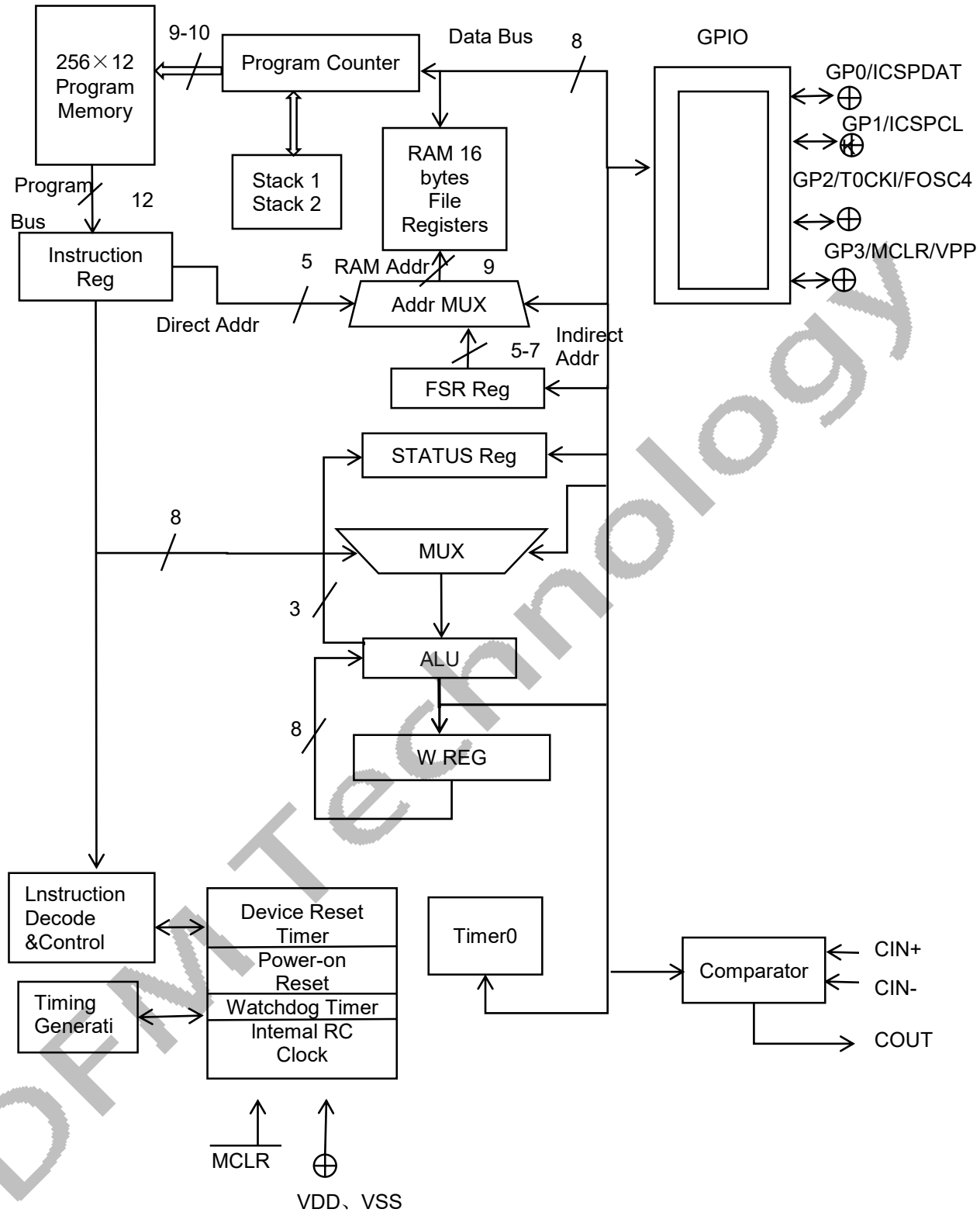


Figure 1.DIF80F222 BLOCK DIAGRAM

Table 3. DIF80F222 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/ICSPDAT/CIN+	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming data pin.
	CIN+	AN	—	Comparator input .
GP1/ICSPCLK/CIN-	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.
	CIN-	AN	—	Comparator input .
GP2/T0CKI/COUT/ FOSC4	GP2	TTL	CMOS	Bidirectional I/O pin.
	T0CKI	ST	—	Clock input to TMR0.
	COUT	—	CMOS	Comparator output .
	FOSC4	—	CMOS	Oscillator/4 output.
$\overline{\text{GP3}}$/$\overline{\text{MCLR}}$/V_{PP}	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as MCLR, this pin is an active-low Reset to the device. Voltage on GP3/MCLR/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as MCLR.
	V_{PP}	HV	—	Programming voltage input.
V_{DD}	V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	P	—	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

Clocking Scheme/Instruction Cycle

The clock is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4.

Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction.

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

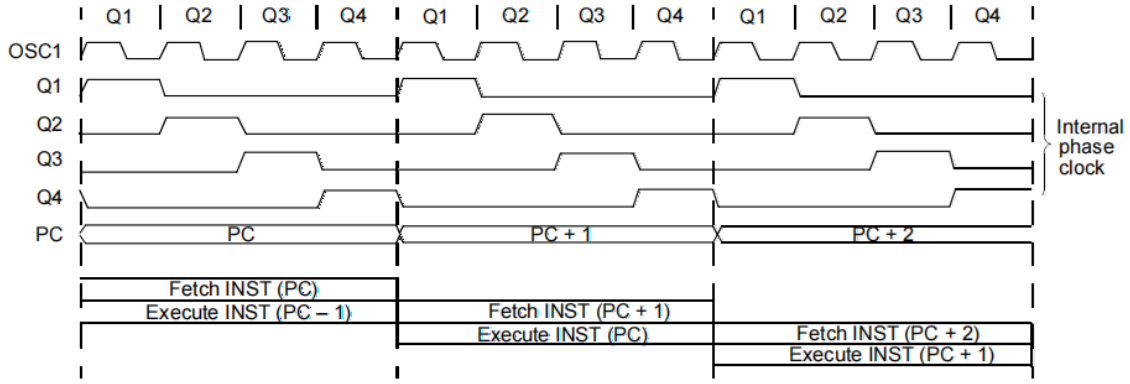
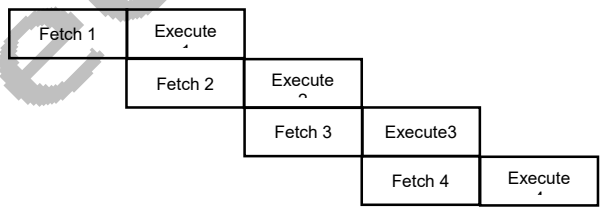


Figure 2.CLOCK/INSTRUCTION CYCLE

EXAMPLE:

```
1.CLRF    02h
2.CLRW
3.CLRF    GPIO
4.BSF     GPIO,BIT1
```



All instructions are single cycle,except for any program branches. These take two cycles, since the fetch instructionis "flushed" from the pipeline, while the new instruction is being fetched and then executed.

MEMORY ORGANIZATION

The DIF80F222 memories are organized into program memory and data memory. Data memory banks are accessed using the File Select Register (FSR).

Program Memory Organization for the DIF80F222

The DIF80F222 devices have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space.

Only the first 256 x 12 (0000h-00FFh) for the DIF80F222 are physically implemented . Accessing a location above these boundaries will cause a wraparound within the first 256 x 12 space (DIF80F222). The effective Reset vector is at 0000h. Location 00FFh (DIF80F222) contains the internal clock oscillator calibration value. This value should never be overwritten.

Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

The Special Function Registers include the TMR0 register, the Program Counter (PCL), the Status register, the I/O register (GPIO) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the DIF80F222, the register file is composed of 7 Special Function Registers and 16 General Purpose Registers.

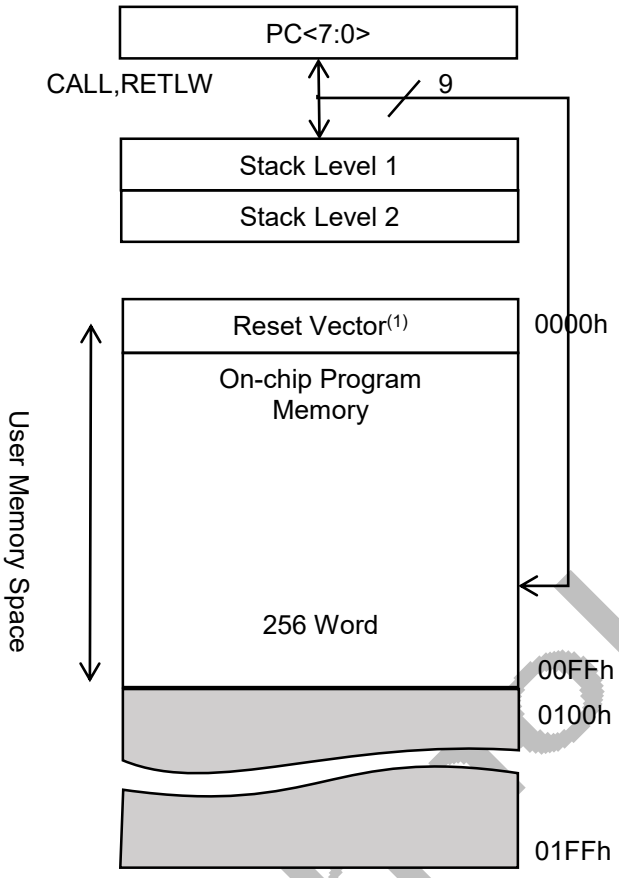


Figure 3.PROGRAM MEMORY MAP AND STACK FOR THE DIF80F222

File Address	
00h	INDF(1)
01h	TMR0
02h	PCL
03h	STATUS
04h	FSR
05h	OSCCAL
06h	GPIO
07h	CMCON0(2)
08h	Unimplemented(3)
0Fh	
10h	General Purpose Registers
1Fh	

Note 1: Not a physical register.

2: DIF80F222 only.

3: Unimplemented, read as 00h.

SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device.

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Table 4.SPECIAL FUNCTION REGISTER (SFR) SUMMARY (DIF80F222)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx
02h(1)	PCL	Low-order 8 bits of PC								1111 1111
03h	STATUS	GPWUF	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	00-1 1xxx(3)
04h	FSR	间接数据存储器地址指针								111x xxxx
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	FOSC4	1111 1110
06h	GPIO	—	—	—	—	GP3	GP2	GP1	GP0	---- xxxx
07h(4)	—	CMPOUT	$\overline{COUTEN}$	POL	$\overline{CMPT0CS}$	CMPON	CNREF	$\overline{CPREF}$	$\overline{CWU}$	---- ----
N/A	TRISGPIO	—	—	—	—	I/O Control Register				---- 1111
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111

Legend: – = unimplemented, read as '0', x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible.

2: Other (NON Power-up) Resets include external Reset through MCLR, Watchdog Timer and wake-up on pin change Reset.

3: Other Reset specific values.

4: DIF80F222 only.

5: DIF80F222 only. On all other devices, this bit is reserved and should not be used.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias..... -40°C to +125°C
Storage temperature..... -65°C to +150°C
Voltage on VDD with respect to VSS.....0 to +6.5V
Voltage on MCLR with respect to VSS.....0 to +13.5V
Voltage on all other pins with respect to VSS.....-0.3V to (VDD + 0.3V)
Total power dissipation(1).....800 mW
Max. current out of VSS pin.....80 mA
Max. current into VDD pin.....80 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > VDD).....±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > VDD).....±20 mA
Max. output current sunk by any I/O pin.....25 mA
Max. output current sourced by any I/O pin.....25 mA
Max. output current sourced by I/O port.....75 mA
Max. output current sunk by I/O port.....75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

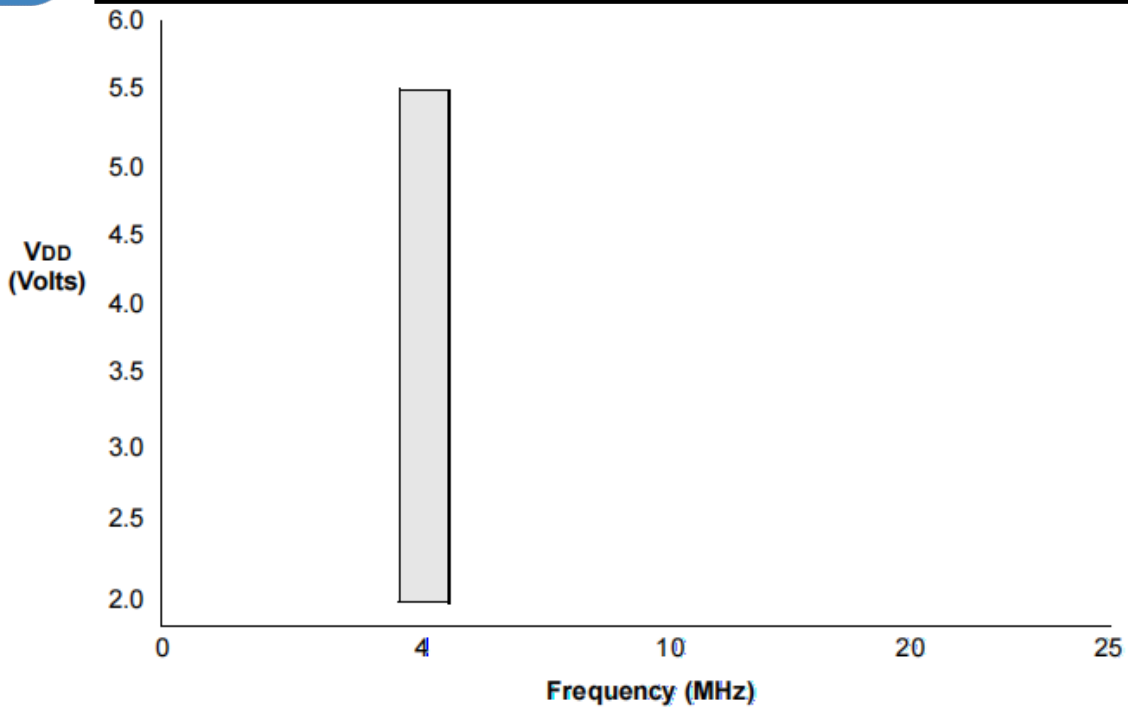


Figure 4. DIF80F222 VOLTAGE-FREQUENCY GRAPH,-40℃ ≤ TA ≤ +125℃

DC Characteristics: DIF80F222

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40 C TA +85 C (industrial)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	
D010	IDD	**Supply Current(3)**	— —	170 350	TBD TBD	μA μA	VDD = 2.0V VDD = 5.0V
D020	IPD	**Power-down Current(4)**	—	0.1	TBD	μA	VDD = 2.0V VDD = 5.0V
D022	ΔIWDT	**WDT Current(4)**	—	1.0	TBD	μA	VDD = 2.0V VDD = 5.0V
D023	ΔICMP	**Comparator Current(4)**	—	15	TBD	μA	VDD = 2.0V VDD = 5.0V
D024	ΔIVREF	**Internal Reference Current(4)**	—	TBD	TBD	μA	VDD = 2.0V VDD = 5.0V

Legend: TBD = To Be Determined.

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25° C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

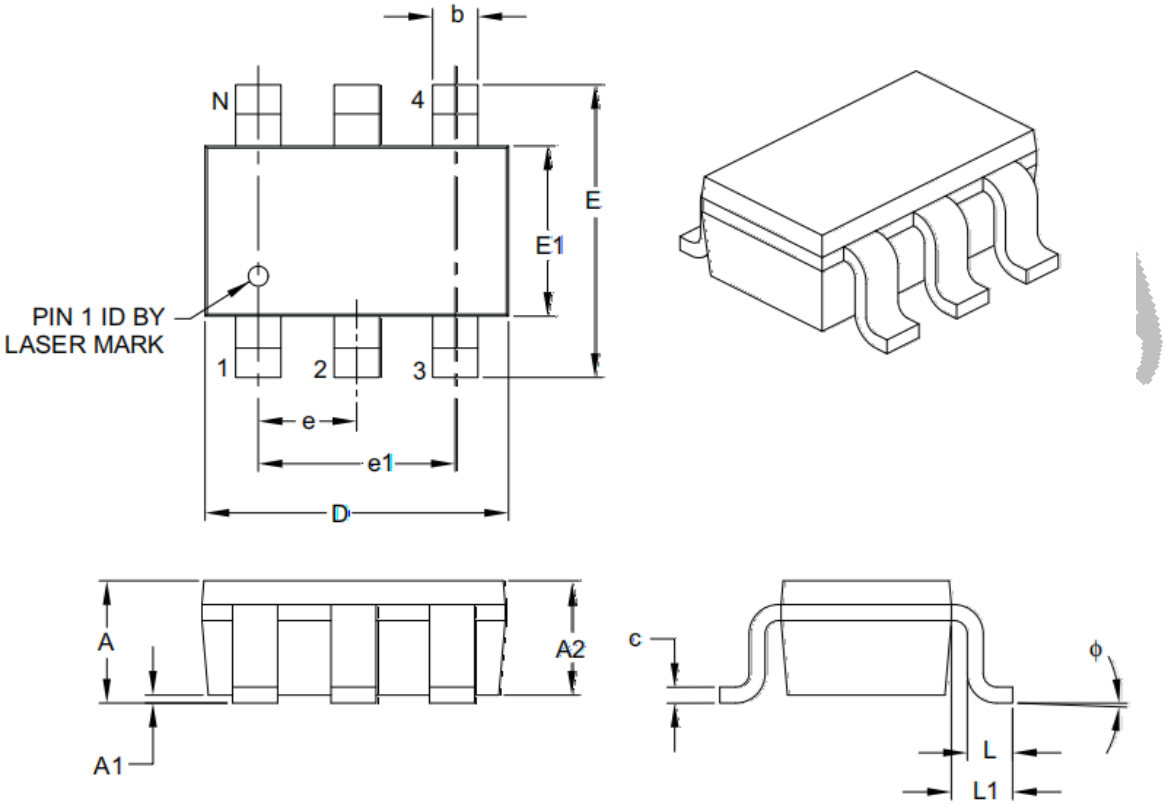
3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a. The test conditions for all IDD measurements in active Operation mode are:All I/O pins tri-stated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
b. For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

Package Details

DIF80F222UI, 6-Lead Plastic Small Outline Transistor (CH or OT) (SOT-23)



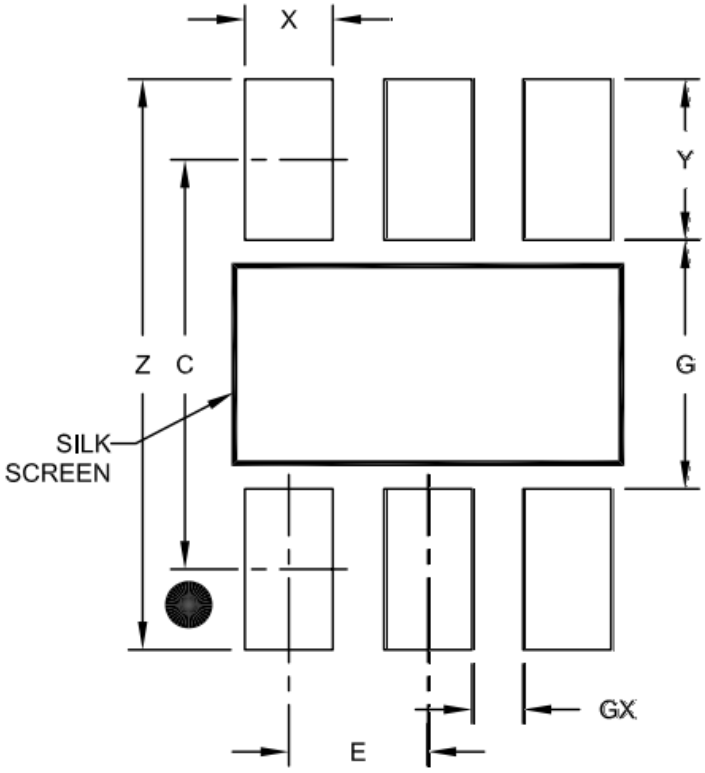
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95BSC	
Outside Lead Pitch	e1		1.90BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.20	-	3.20
Molded Package Width	E1	1.30	-	1.80
Overall Length	D	2.70	-	3.10
Foot Length	L	0.10	-	0.60
Footprint	L1	0.35	-	0.80
Foot Angle	ϕ	0°		30°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF80F222UI, 6-Lead Plastic Small Outline Transistor (CH or OT) (SOT-23)



RECOMMENDED LAND PATTERN

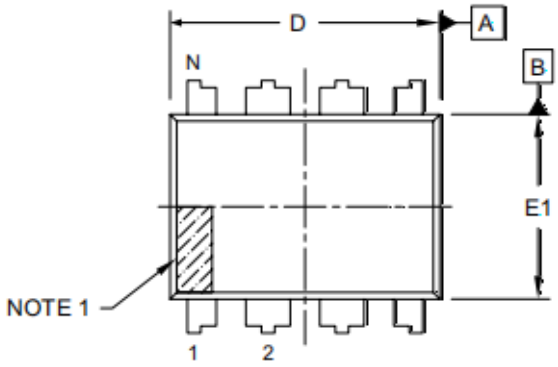
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width(X6)	X			0.60
Contact Pad Length(X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	Gx	0.35		
Overall Width	Z			3.90

Notes:

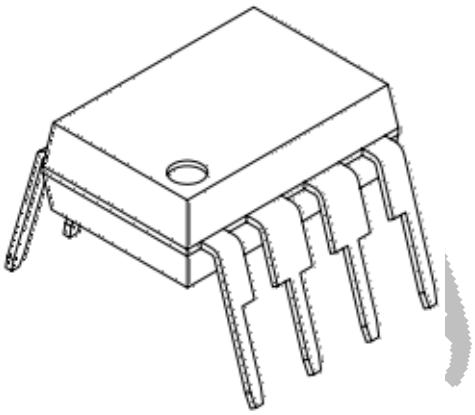
1. Dimensioning and tolerancing per ASME Y14.5M.

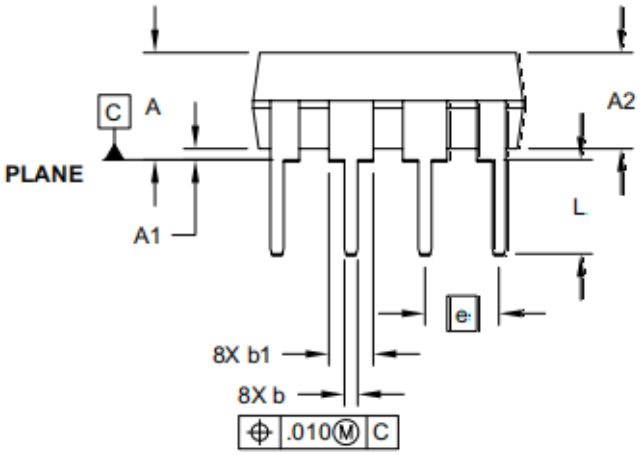
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

DIF80F222DI, 8-Lead Plastic Dual In-line (P) – 300 mil (DIP)

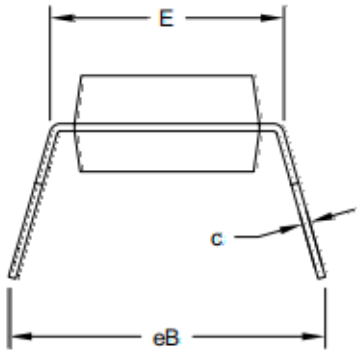


TOP VIEW



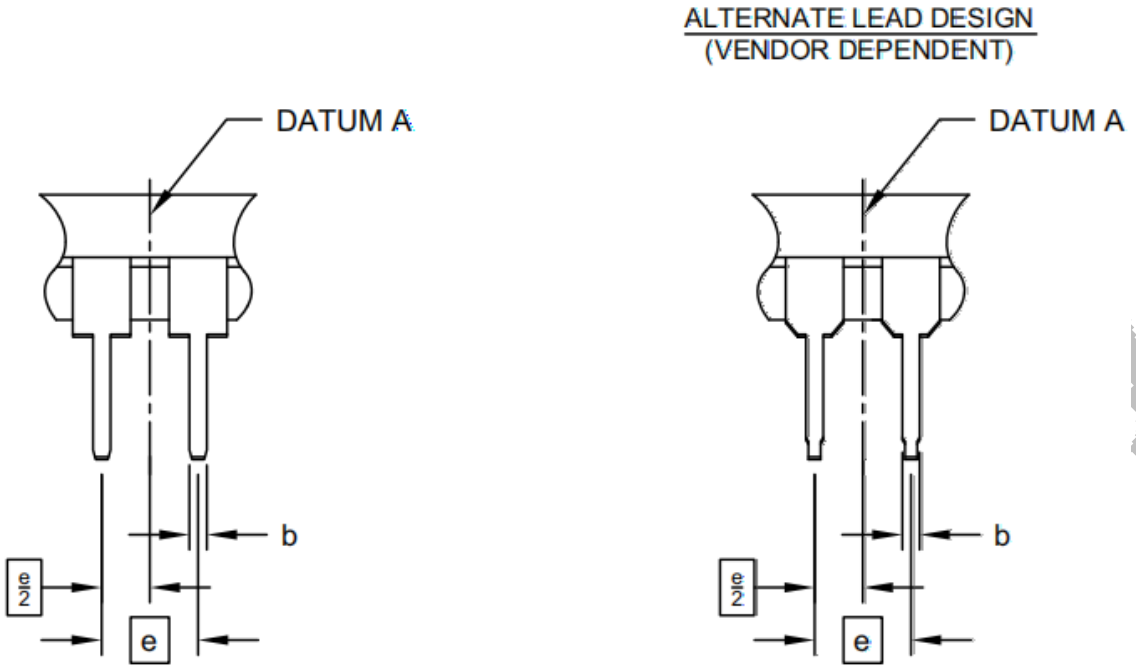


SIDE VIEW



END VIEW

DIF80F222DI, 8-Lead Plastic Dual In-line (P)-300 mil (DIP)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed.010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.