Difmicro Technology

DIF6001/2/4

Datasheet

CONTENTS

1 MHz, Low-Power Op Amp

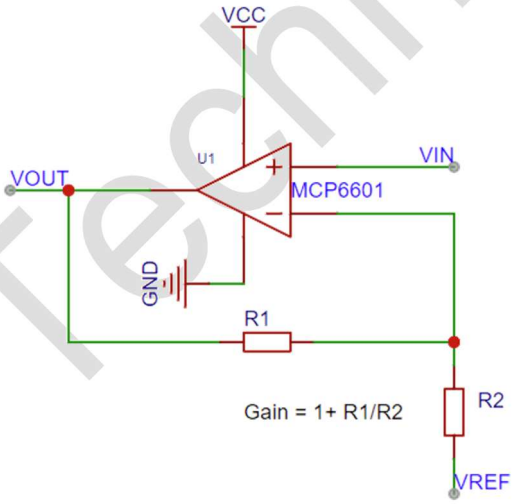
Features

- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typ.)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 5.5V
- Supply Current: IQ = 100 µA (typ.)
- Phase Margin: 90° (typ.)
- Temperature Range:
- Industrial: -40°C to +85°C
- Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Typical Application



Description

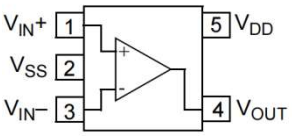
The Difmicro Technology Inc. DIF6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typ.). It also maintains 45° phase margin (typ.) with a 500pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100µA (typ.) quiescent current. Additionally, the DIF6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of VDD + 300mV to VSS – 300mV. This family of op amps is designed with Difmicro's advanced CMOS process.

The DIF6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 5.5V.

Package Types

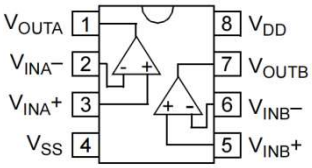
DIF6001

SOT-23-5



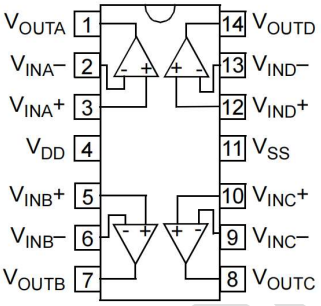
DIF6002

PDIP, SOIC, MSOP



DIF6004

PDIP, SOIC, TSSOP



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

VDD – VSS 7.0V

All Inputs and Outputs ..... VSS – 0.3V to VDD + 0.3V

Difference Input Voltage ..... |VDD – VSS|

Output Short-Circuit Current .....continuous

Current at Input Pins .....±2mA

Current at Output and Supply Pins .....±30mA

Storage Temperature.....-65° C to +150° C

Maximum Junction Temperature (TJ).....+150° C ESD Protection On All Pins (HBM;MM) ..... ⩾ 4kV; 200V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and V_{OUT} ≈ V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	V_{CM} = V_{SS} **(Note 1)**
Input Offset Drift with Temperature	⊗V_{OS}/⊗T_A	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, V_{CM} = V_{SS}
Power Supply Rejection Ratio	PSRR	—	86	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
Industrial Temperature	I_B	—	19	—	pA	T_A = +85°C
Extended Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	∧||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	∧||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} □ 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{CM} = V_{SS}
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} H V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6.1	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/□Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/□Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Industrial Temperature Range	T_A	-40	—	+85	°C	
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC (150 mil)	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

2.0 PIN DESCRIPTIONS

PIN FUNCTION TABLE

DIF6001	DIF6001R	DIF6001U	DIF6002	DIF6004	Symbol	Description
1	1	4	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	4	3	2	2	V_{IN}–, V_{INA}–	Inverting Input (op amp A)
3	3	1	3	3	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	V_{INB}+	Non-inverting Input (op amp B)
—	—	—	6	6	V_{INB}–	Inverting Input (op amp B)
—	—	—	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	9	V_{INC}–	Inverting Input (op amp C)
—	—	—	—	10	V_{INC}+	Non-inverting Input (op amp C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	V_{IND}+	Non-inverting Input (op amp D)
—	—	—	—	13	V_{IND}–	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)

Analog Outputs

The output pins are low-impedance voltage sources.

Analog Inputs

The non-inverting and inverting inputs are high- impedance CMOS inputs with low bias currents.

Power Supply (VSS and VDD)

The positive power supply (VDD) is 1.8V to 5.5V higher than the negative power supply (VSS). For normal operation, the other pins are at voltages between VSS and VDD .

Typically, these parts are used in a single (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply. VDD will need a local bypass capacitor (typically 0.01 µF to0.1 µF) within 2 mm of the VDD pin. These parts can share a bulk capacitor with analog parts (typically 2.2µF to 10µF) within 100 mm of the VDD pin.

3.0 APPLICATION INFORMATION

The DIF6001/2/4 family of op amps is manufactured using Difmicro’s state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the DIF6001/2/4 ideal for battery-powered applications.

3.1 Rail-to-Rail Input

The DIF6001/2/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows the input voltage exceeding the supply voltage without any phase reversal.

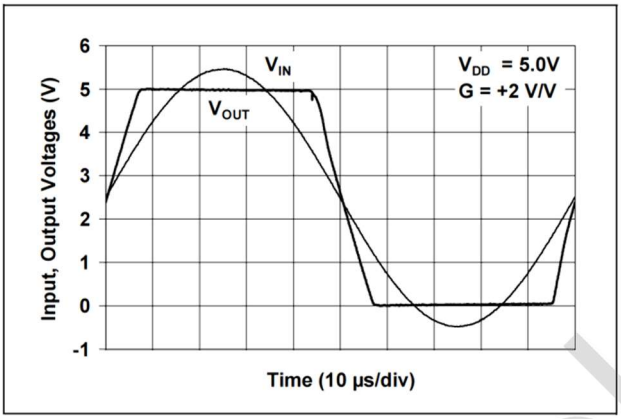
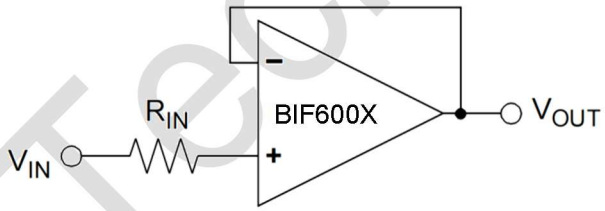


FIGURE 3-1: The DIF6001/2/4 Show No Phase Reversal.

The input stage of the DIF6001/2/4 op amps use two differential input stages in parallel. One operates at a low common mode input voltage (VCM), while the other operates at a high VCM. With this topology, the device operates with a VCM up to 300 mV above VDD and 300 mV below VSS. The input offset voltage is measured at VCM = VSS – 300 mV and VDD + 300 mV to ensure proper operation.

Input voltages that exceed the input voltage range (VSS – 0.3V to VDD + 0.3V at 25° C) can cause excessive current to flow into or out of the input pins, while current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 3-2.



$$R_{IN} \geq \frac{(Maximum\ expected\ V_{IN}) - V_{DD}}{2\ mA}$$

$$R_{IN} \geq \frac{V_{SS} - (Minimum\ expected\ V_{IN})}{2\ mA}$$

FIGURE 3-2: Input Current Limiting Resistor (RIN).

3.2 Rail-to-Rail Output

The output voltage range of the DIF6001/2/4 op amps is VDD – 25 mV(min.) and VSS + 25 mV (max.) when RL = 10kΩ is connected to VDD/2 and VDD = 5.5V.

3.3 Capacitive Loads

Driving large capacitive loads can cause stability prob- lems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response,with overshoot and ringing in the step response. While a unity-gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (RISO in Figure 3-3) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The band- width will be generally lower than the bandwidth with no capacitance load.

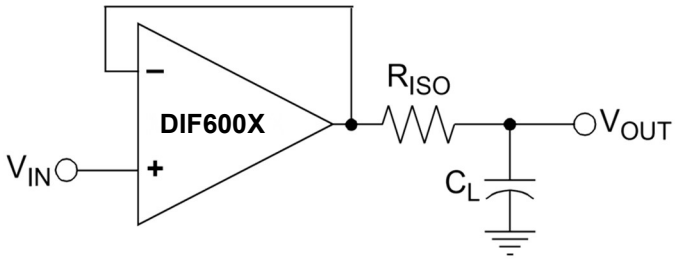


FIGURE 3-3: Output resistor, RISO stabilizes large capacitive loads.

Figure 3-4 gives recommended RISO values for different capacitive loads and gains. The x-axis is the normalized load capacitance (CL/GN), where GN is the circuit's noise gain. For non-inverting gains, GN and the Signal Gain are equal. For inverting gains, GN is 1+|Signal Gain| (e.g., -1 V/V gives GN = +2 V/V).

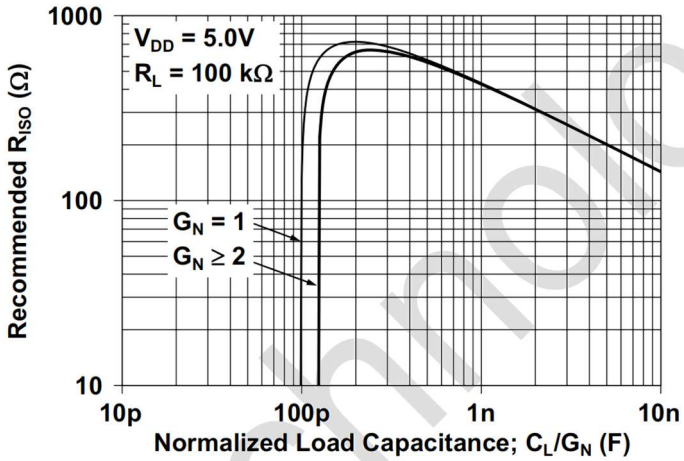


FIGURE 3-4: Recommended RISO values for Capacitive Loads.

After selecting RISO for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify RISO's value until the response is reasonable. Bench evaluation and simulations with the DIF6001/2/4 SPICE macro model are very helpful.

3.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (VDD for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

3.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 1012Ω. A 5V difference would cause 5pA of current to flow; which is greater than the DIF6001/2/4 family's bias current at 25°C (1pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-5.

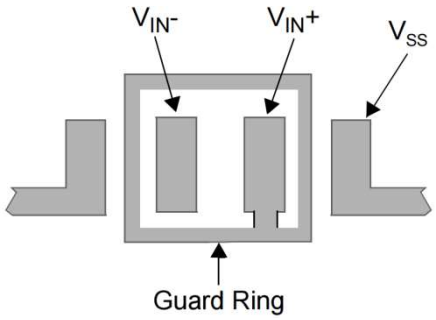


FIGURE 3-5: Example Guard Ring Layout for Inverting Gain

1.Non-inverting Gain and Unity-Gain Buffer:

a.Connect the non-inverting pin (VIN+) to the input with a wire that does not touch the PCB surface.

b.Connect the guard ring to the inverting input pin (VIN–). This biases the guard ring to the common mode input voltage.

2.Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):

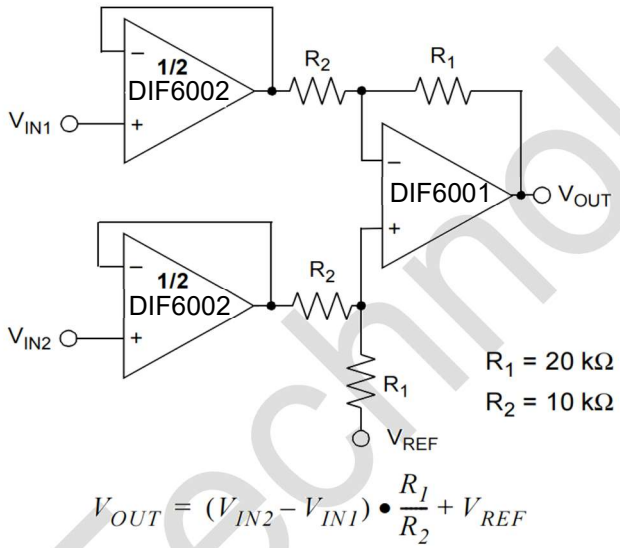
a.Connect the guard ring to the non-inverting input pin (VIN+). This biases the guard ring to the same reference voltage as the op amp (e.g., VDD/2 or ground).

b.Connect the inverting pin (VIN–) to the input with a wire that does not touch the PCB surface.

3.6 Application Circuits

3.6.1 UNITY-GAIN BUFFER

The rail-to-rail input and output capability of the DIF6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 3-6.



$$V_{OUT} = (V_{IN2} - V_{IN1}) \bullet \frac{R_1}{R_2} + V_{REF}$$

FIGURE 3-6: Instrumentation Amplifier with Unity-Gain Buffer Inputs.

3.6.2 ACTIVE LOW-PASS FILTER

The DIF6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resis- tors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the fre- quency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100X the filter cutoff frequency (or higher) for good performance. It is possi- ble to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 3-7 shows a second-order Butterworth filter with100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10X higher than the cutoff frequency. The component values were selected using Difmicro's FilterLab® software.

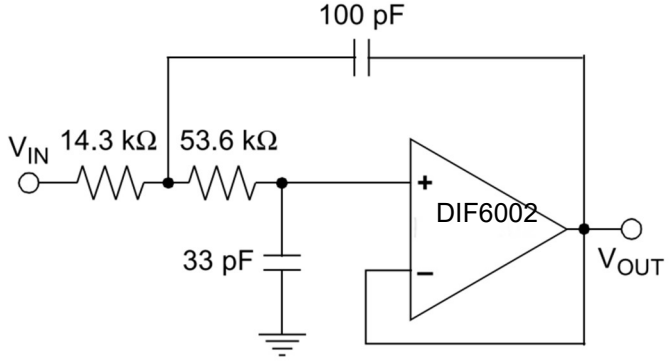


FIGURE 3-7:Active Second-Order Low- Pass Filter.

3.6.3 PEAK DETECTOR

The DIF6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applica- tions. Figure 3-8 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 3-8.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch.When the Clear Switch closes, C_1 discharges through R_1 for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT}.

In order to define tSAMP and tCLEAR, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R1 (τ = R1C1). tDETECT is the time that the input signal is sampled on C1 and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors(both C1 and C2), could create slewing limitations as the input voltage(VIN)increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short- circuit current of ISC = 25 mA and a load capacitor of C1 = 0.1 µF, then:This voltage rate of change is less than the DIF6001/2/4 slew rate of 0.6 V/µs. When the input voltage swings below the voltage across C_1, D_1 becomes reverse- biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capaci- tors should be less than 40 µF and a stabilizing resistor (R_{ISO}) needs to be properly selected.

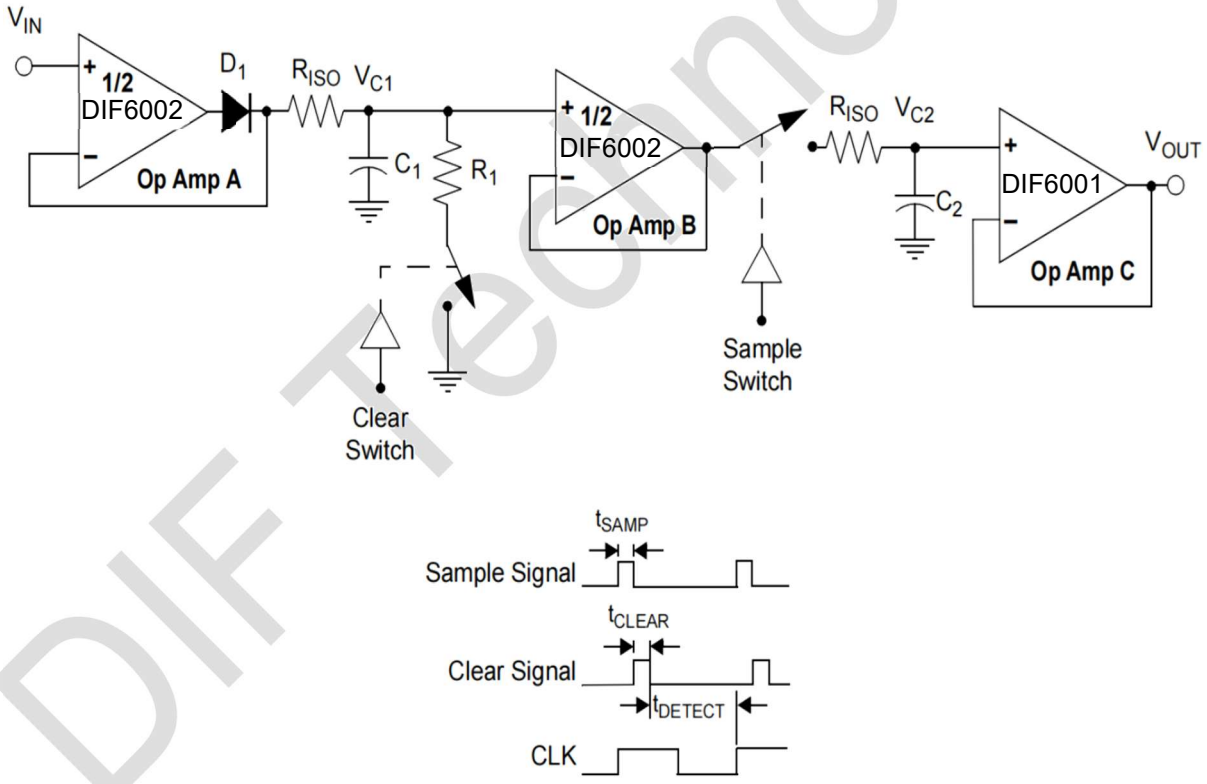
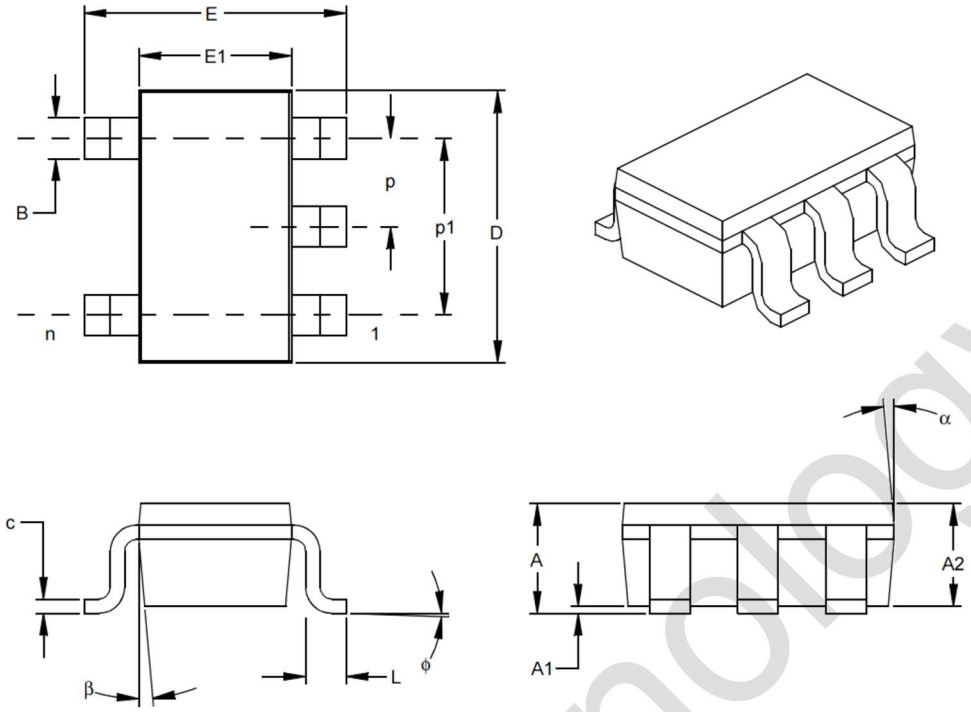


FIGURE 3-8: Peak Detector with Clear and Sample CMOS Analog Switches.

4.0 Package Marking Information

5-Lead Plastic Small Outline Transistor (OT) (DIF6001UI)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	⟩	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	⟨	0	5	10	0	5	10
Mold Draft Angle Bottom	®	0	5	10	0	5	10

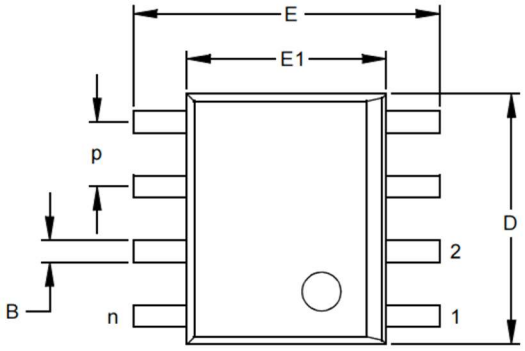
* Controlling Parameter

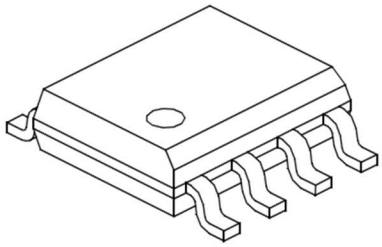
§ Significant Characteristic

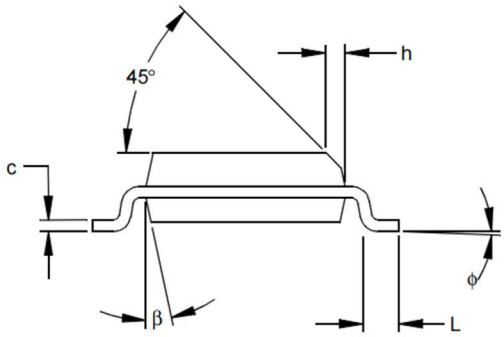
Notes:

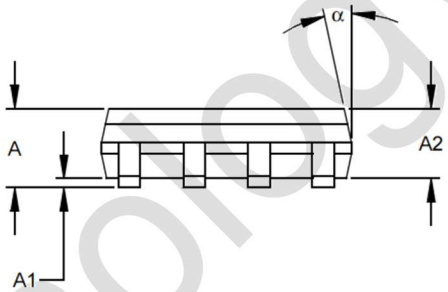
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.

8-Lead Plastic Small Outline (DIF6002SI) – Narrow, 150 mil









Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	)	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	(	0	12	15	0	12	15
Mold Draft Angle Bottom	®	0	12	15	0	12	15

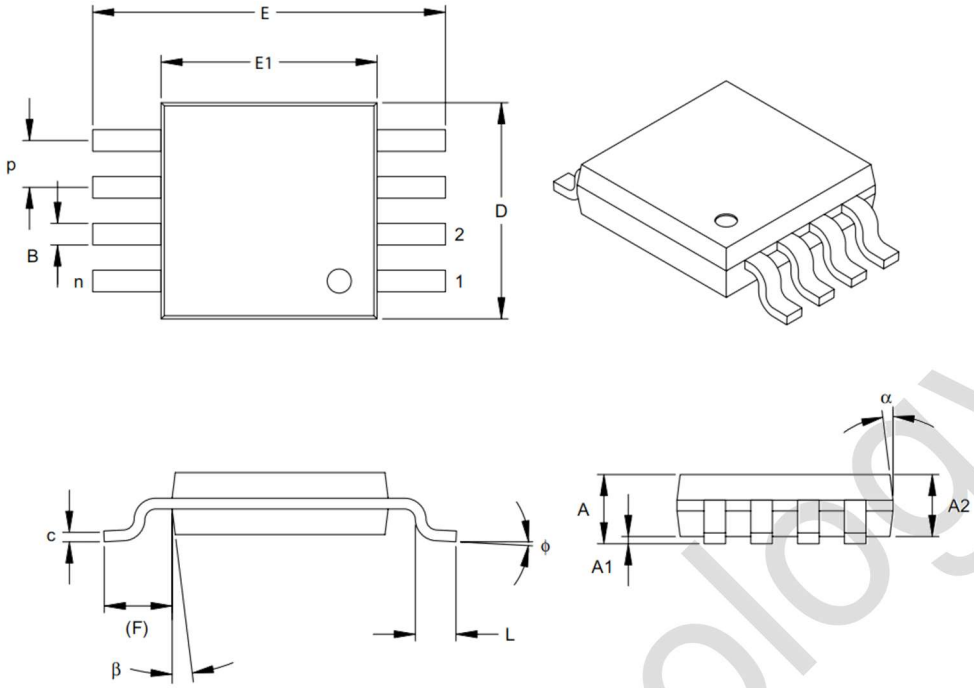
* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.

8-Lead Plastic Micro Small Outline Package (DIF6002MI)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	⟩	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	⟨	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	®	5°	-	15°	5°	-	15°

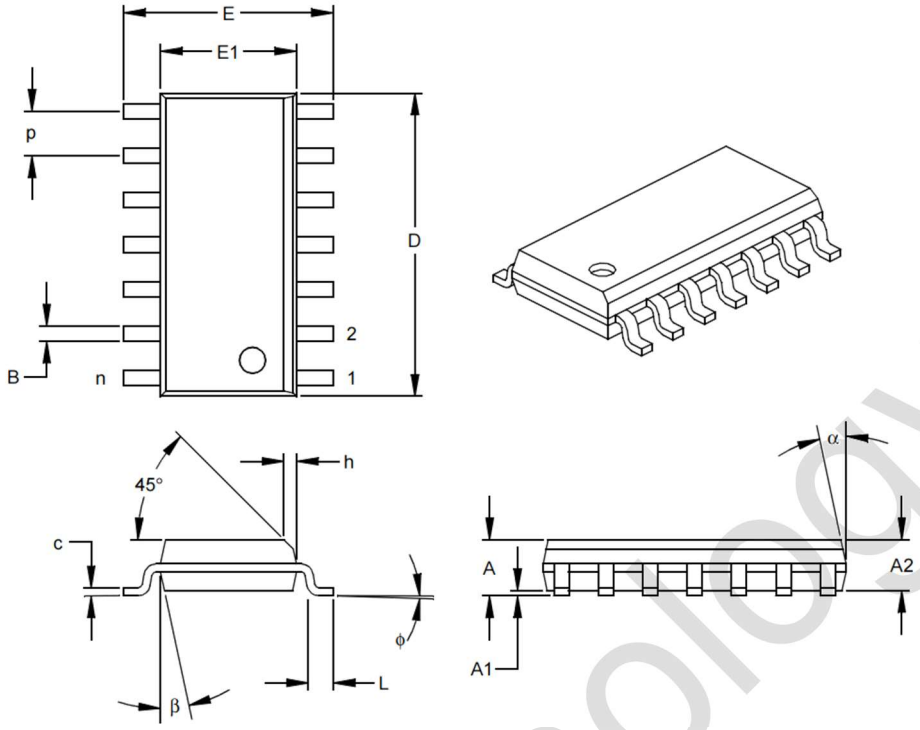
* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.

14-Lead Plastic Small Outline (DIF6004SI) – Narrow, 150 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	\	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	〈	0	12	15	0	12	15
Mold Draft Angle Bottom	®	0	12	15	0	12	15

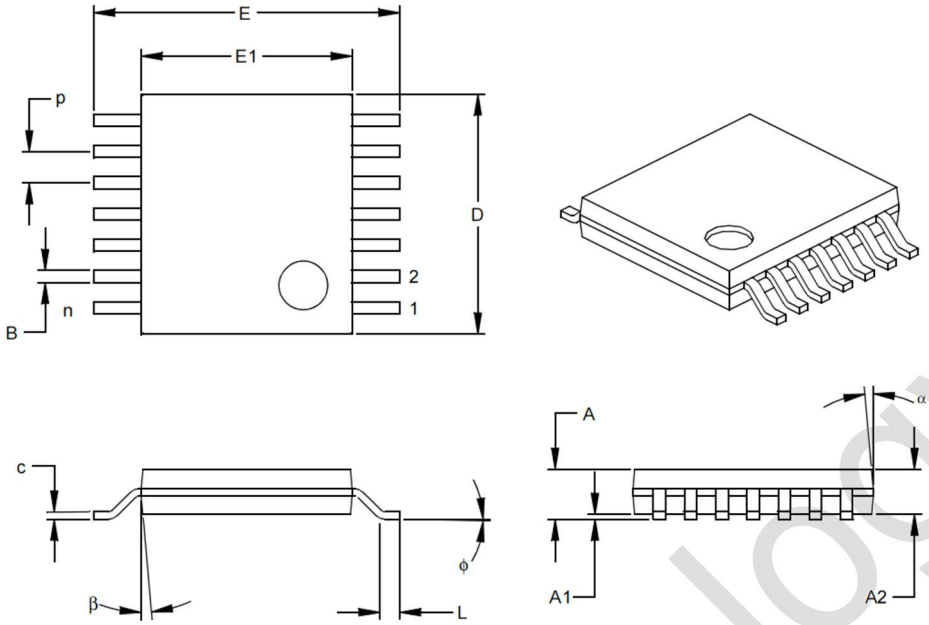
* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.

14-Lead Plastic Thin Shrink Small Outline (DIF6004TI) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.